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LEA-5
u-blox 5 GPS and GALILEO Modules
Hardware Integration Manual
(incl. Reference Design)

Abstract

This document describes the hardware features and specifications of the u-blox 5 based LEA-5 series of cost effective, high-performance GPS/GALILEO modules.

Features include AssistNow Online and AssistNow Offline A-GPS services, KickStart accelerated acquisition, SuperSense® Indoor GPS providing best-in-class acquisition and tracking sensitivity, precision timing and an innovative jamming-resistant RF architecture. The compact 17.0 x 22.4 mm form factor of the highly successful LEA-4 series is maintained, enabling easy migration. The LEA-5 series supports passive and active antennas.

A Reference Design is included and guides through the design-in of a LEA-5 module.

your position is our focus

Manual

Title	LEA-5	
Subtitle	Hardware Integration Manual	(incl. Reference Design)
Doc Type	Manual	Preliminary
Doc Id	GPS.G5-MS5-07005 A3	

Revision Index	Date	Name	Status / Comments
Initial Version	18/01/2008	TC	
Initial Release	20/02/2008	TG	Addition of Hardware Description, Product Handling, Product Testing, Appendix
A	19/03/2008	TG	Addition of Reference Design. Update to include Eco Power Mode
A1	23/04/2008	TG	USB update
A2	12/11/2008	TG	Module Selector, Power Modes, USB, DDC, SPI, Design-in Checklist, ESD Precautions, Migration Tables: Vbckp, Vant
A3	12/12/2008	TG	DDC, Design in recommendations

	Products marked with this lead-free symbol on the product label comply with the "Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).
	This is an Electrostatic Sensitive Device (ESD). Observe precautions for handling.

Preface

u-blox Technical Documentation

As part of our commitment to customer support, u-blox maintains an extensive volume of technical documentation for our products. In addition to our product-specific technical data sheets, the following manuals are available to assist u-blox customers in product design and development.

- **GPS Compendium:** This document, also known as the GPS book, provides a wealth of information regarding generic GPS questions about system functionalities and technology.
- **Protocol Specification:** Messages, configuration and functionalities of the u-blox 5 software releases are explained in this document.
- **Hardware Integration Manual:** This Manual provides hardware design instructions and information on how to set up production and final product tests.
- **Application Note:** document provides general design instructions and information that applies to all u-blox GPS receivers. See Section **Related Documents** for a list of Application Notes related to your GPS receiver.

How to use this Manual

The LEA-5 Hardware Integration Manual provides the necessary information to successfully design in and configure these u-blox 5-based GPS/GALILEO receiver modules. For navigating this document please note the following:

This manual has a modular structure. It is not necessary to read it from the beginning to the end. To help in finding needed information, a brief section overview is provided below:

1. **Hardware Description**: This chapter introduces the basics of function and architecture of the LEA 5 modules.
2. **Design-In**: This chapter provides the Design-In information necessary for a successful design.
3. **Product Handling**: This chapter defines packaging, handling, shipment, storage and soldering.
4. **Product Testing**: This chapter provides information about testing of OEM receivers in production.
5. **Appendix:** The Appendix includes a Reference Design, guidelines on how to successfully migrate to u-blox 5 designs, and useful information about the different antenna types available on the market and how to reduce interference in your GPS design.

The following symbols are used to highlight important information within the manual:

☞ An index finger points out key information pertaining to module integration and performance.

⚠ **A warning symbol indicates actions that could negatively impact or damage the module.**

Questions

If you have any questions about u-blox 5 Hardware Integration, please:

- Read this manual carefully.
- Contact our information service on the homepage http://www.u-blox.com
- Read the questions and answers on our FAQ database on the homepage http://www.u-blox.com

Technical Support

Worldwide Web

Our website (www.u-blox.com) is a rich pool of information. Product information, technical documents and helpful FAQ can be accessed 24h a day.

By E-mail

If you have technical problems or cannot find the required information in the provided documents, contact the nearest of the Technical Support offices by email. Use our service pool email addresses rather than any personal email address of our staff. This makes sure that your request is processed as soon as possible. You will find the contact details at the end of the document.

Helpful Information when Contacting Technical Support

When contacting Technical Support please have the following information ready:

- Receiver type (e.g. LEA-5A) and firmware version (e.g. V4.00)
- Receiver configuration
- Clear description of your question or the problem together with a u-center logfile
- A short description of the application
- Your complete contact details

Contents

1 Hardware Description

1.1 Functional Overview

The LEA-5 module series is a family of self-contained GPS and GALILEO receivers featuring the powerful 50-channel u-blox 5 positioning engine. These modules provide exceptional GPS performance in a compact form factor and at an economical price. u-blox 5 sets a new standard in GPS receiver technology. A 32-channel acquisition engine with over 1 million effective correlators is capable of massive parallel searches across the time/frequency space. This enables a Time To First Fix (TTFF) of less than 1 second, while long correlation/dwell times make possible the best-in-class acquisition and tracking sensitivity. Once acquired, satellites are passed on to a dedicated tracking engine. This arrangement allows the GPS engine to simultaneously track up to 16 satellites while searching for new ones. u-blox 5's advanced jamming suppression mechanism and innovative RF architecture provide a high level of immunity to jamming, ensuring maximum GPS performance. u-blox 5 has been designed to be able to support the GALILEO system currently being developed by European authorities. The capability of receiving GALILEO L1 signals will provide increased coverage and even better positioning accuracy when this system comes into operation.

With the LEA-5 series the complete signal processing chain from antenna input to serial output is contained within a single component. LEA-5 modules maintain the compact 17.0 x 22.4 mm form factor of their highly successful LEA-4 predecessors. The LEA-5 modules have been designed with backwards compatibility in mind, enabling ease of upgrade and reducing engineering and design costs.

Their small size makes LEA-5 modules the ideal GPS solution for applications with stringent space requirements. The packaging makes expensive RF cabling obsolete, with the RF input being available directly on a pin. The LEA-5 series are SMT solderable and can be handled by standard pick and place equipment.

LEA-5 modules come equipped with a serial port, which can handle NMEA and UBX proprietary data formats, as well as a high speed USB port. The optional FLASH Memory provides the capacity to store user-specific configuration settings as well as future software updates. All LEA-5 modules are RoHS compliant (lead-free).

The LEA-5 series of GPS/GALILEO receiver modules are not designed for life saving or supporting devices or for aviation and should not be used in products that could in any way negatively impact the security or health of the user or third parties or that could cause damage to goods.

1.2 Module Selector

u-blox provides several modules using the popular and industry standard LEA Form factor. To select the right product for your design consider Table 1:

	Voltage Range (V)	Thickness (mm)	50-channel engine	KickStart	SuperSense	FW Update / FLASH	Low Power Modes	UART	USB	SPI	DDC	AssistNow Online	AssistNow Offline	Dead Reckoning	Raw Data	Precision Timing	1PPS	CFG Pins	Reset Input	Antenna Supply	Antenna Supervisor
LEA-5H	**2.7-3.6**	**3.0**	✓	✓	✓	✓	**P**	**1**	**1**		**1**	✓	✓				✓		✓	✓	✓
LEA-5S	**2.7-3.6**	**3.0**	✓	✓	✓		**P**	**1**	**1**[1]		**1**	✓	✓				✓	**1**	✓	✓	✓
LEA-5A	**2.7-3.6**	**3.0**	✓		✓		**P**	**1**	**1**[2]		**1**	✓	✓				✓	**1**	✓	✓	✓
LEA-5Q	**2.7-3.6**	**2.4**	✓	✓	✓		**P**	**1**	**1**	**1**	**1**	✓	✓				✓	**3**	✓		
LEA-5M	**2.7-3.6**	**2.4**	✓		✓		**P**	**1**	**1**		**1**	✓	✓				✓	**2**	✓		
LEA-5T	**2.7-3.6**	**3.0**	✓	✓	✓		**P**	**1**	**1**		**1**	✓	✓			✓	✓		✓	✓	✓

P= Planned

Table 1: Features of the LEA-5 Series

1.3 Architecture

LEA-5 modules are divided into two functional sections. The smaller section is the RF- Section, the larger section contains the Baseband. See Figure 1 for a block diagram of the LEA-5 series.The RF Front-End contains the integrated Low Noise Amplifier (LNA), the SAW bandpass filter, the u-blox 5 RF-IC and the TCXO or XTO crystal. The Baseband section contains the digital circuitry comprised of the u-blox 5 Baseband processor, the RTC crystal and additional elements such as the optional FLASH Memory for enhanced programmability and flexibility.

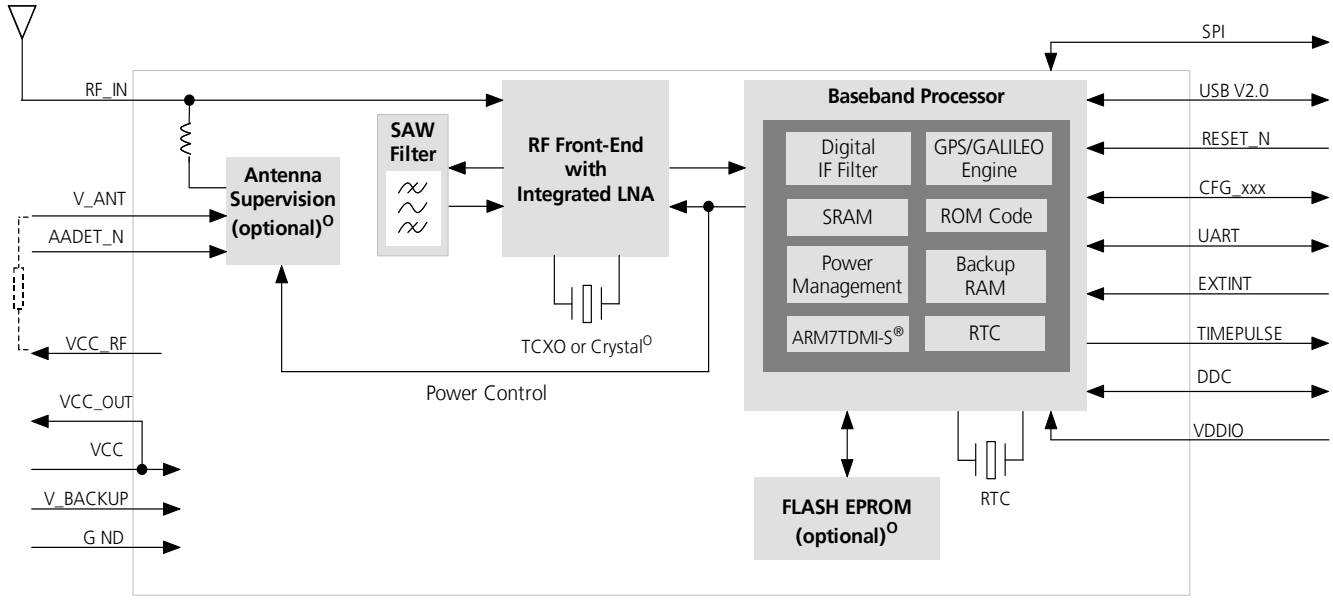


Figure 1: LEA-5 Block Diagram
O: For available options refer to the product features table in section 1.2.

[1] Supported by LEA-5S-0-003 and above.
[2] Supported by LEA-5A-0-003 and above.

2 Design-In

☞ For migrating existing ANTARIS®4 product designs to u-blox 5 please refer to *Appendix A*.

In order to obtain good performance with a GPS receiver module, there are a number of points that require careful attention during the design-in. These include:

- Power Supply
  Good performance requires a clean and stable power supply.
- Interfaces
  Ensure correct wiring, rate and message setup on the module and your host system.
- Antenna interface
  For optimal performance seek short routing, matched impedance and no stubs.

2.1 Power Management

2.1.1 Connecting Power

u-blox 5 receivers have three power supply pins: **VCC**, **V_BCKP** and **VDDUSB**.

2.1.1.1 VCC - Main Power

The main power supply is fed through the **VCC** pin. During operation, the current drawn by the u-blox 5 GPS module can vary by some orders of magnitude, especially, if low-power operation modes are enabled. It is important that the system power supply circuitry is able to support the peak power (see datasheet for specification) for a short time. In order to define a battery capacity for specific applications the sustained power figure shall be used.

2.1.1.2 V_BCKP - Backup Battery

In case of a power failure on pin **VCC**, the real-time clock and backup RAM are supplied through pin **V_BCKP**. This enables the u-blox 5 receiver to recover from a power failure with either a Hotstart or a Warmstart (depending on the duration of **VCC** outage) and to maintain the configuration settings. If no backup battery is connected, the receiver performs a Coldstart at power up.

☞ If no backup battery available connect the **V_BCKP** pin to **GND (or VCC)**.

As long as **VCC** is supplied to the u-blox 5 receiver, the backup battery is disconnected from the RTC and the backup RAM in order to avoid unnecessary battery drain (see Figure 2). Power to RTC and BBR is supplied from **VCC** in this case.

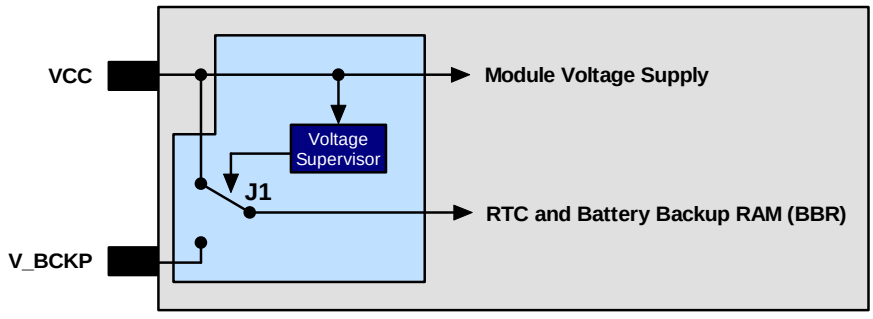


Figure 2: Backup Battery and Voltage

2.1.1.3 VDD_USB - USB Interface Power Supply

VDD_USB supplies the I/Os of the USB interface. If the USB interface is not used, the **VDD_USB** pin must be connected to GND. For more information regarding the correct handling of **VDD_USB** see section 2.3.2.1

2.1.2 Power Modes

u-blox 5 technology offers power optimized architecture with built-in autonomous power saving functions that minimize power consumption at any given time.

u-blox 5 can be operated in two different power modes: Maximum Performance and Eco Mode. In both cases, the receiver is operated in continuous mode. The difference lies in how the acquisition engine is used. Maximum Performance Mode freely uses the acquisition engine, resulting in the best possible TTFF at weak signals. With Eco Mode the use of the acquisition engine is optimized to deliver lower current consumption.

Low Power Modes are planned.

For more information, see the *u-blox 5 Protocol Specification* [1].

2.1.3 V_ANT

LEA-5 modules supporting active antenna supply and supervision use the pin **V_ANT** to supply the active antenna. Use a 10R resistor in front of **V_ANT**[3]. See chapter 2.9.

2.2 System Functions

2.2.1 EXTINT - External Interrupt Pin

EXTINT0 is an external interrupt pin. It is used for the time mark function on LEA-5T and will be used in future LEA-5 releases for wake-up functions in low-power modes.

2.2.2 System Monitoring

The u-blox 5 GPS and GALILEO Receiver provides System Monitoring functions that allow the operation of the embedded processor and associated peripherals to be supervised. These System Monitoring functions are being output as part of the UBX protocol, class 'MON'.

Please refer to the *u-blox 5 Protocol Specification [1]*. For more information on UBX messages, serial interfaces for design analysis and individual system monitoring functions.

2.3 Interfaces

2.3.1 Serial

UART 1 (**RxD1/TxD1**) is the default serial interface. It supports data rates from 4.8 to 230.4 kBit/s. The signal output levels are 0 V to VCC (or VDDIO where available). An interface based on RS232 standard levels (+/- 12 V) can be realized using level shifters such as Maxim MAX3232.

☞ The **RxD1** has fixed input voltage thresholds, which do not depend on **VCC** (see *LEA-5 Data Sheet* [3]). Leave open if unused.

Hardware handshake signals and synchronous operation are not supported.

For the default settings see the *LEA-5 Data Sheet* [3].

[3] Only applies to LEA-5 modules supporting active antenna supply and supervision.

2.3.2 USB

The u-blox 5 USB interface supports the full-speed data rate of 12 Mbit/s.

2.3.2.1 USB external components

The USB interface requires some external components in order to implement the physical characteristics required by the USB 2.0 specification. These external components are shown in Figure 3 and listed in Table 2.

In order to comply with USB specifications, VBUS must be connected through a LDO (U1) to pin **VDD_USB** of the module.

If the USB device is **self-powered** it is possible that the power supply (VCC) is shut down and the Baseband-IC core is not powered. Since VBUS is still available, it still would be signaled to the USB host that the device is present and ready to communicate. This is not desired and thus the LDO (U1) should be disabled using the enable signal (EN) of the VCC-LDO or the output of a voltage supervisor. Depending on the characteristics of the LDO (U1) it is recommended to add a pull-down resistor (R11) at its output to ensure **VDD_USB** is not floating if LDO (U1) is disabled or the USB cable is not connected i.e. VBUS is not supplied.

If the device is **bus-powered**, LDO (U1) does not need an enable control.

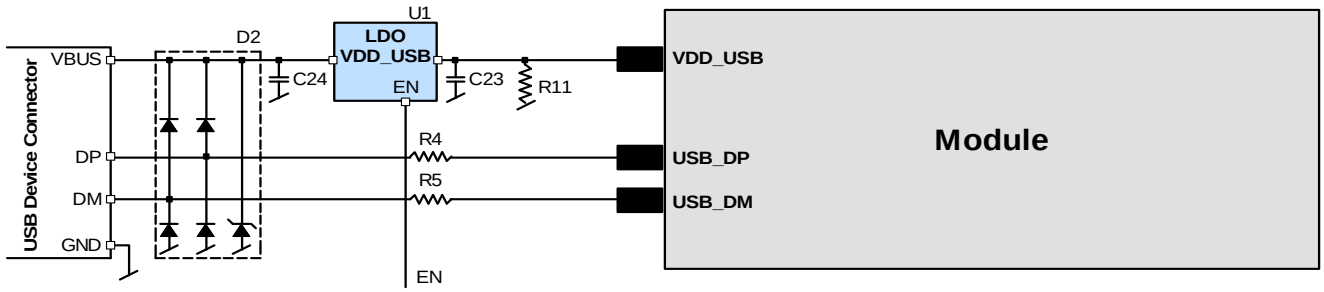


Figure 3: USB Interface

Name	Component	Function	Comments
U1	LDO	Regulates VBUS (4.4 …5.25 V) down to a voltage of 3.3 V).	Almost no current requirement (~1 mA) if the GPS receiver is operated as a USB self-powered device, but if bus-powered LDO (U1) must be able to deliver the maximum current of ~150 mA. A low-cost DC/DC converter such as LTC3410 from Linear Technology may be used as an alternative.
C23, C24	Capacitors		Required according to the specification of LDO U1
D2	Protection diodes	Protect circuit from overvoltage / ESD when connecting.	Use low capacitance ESD protection such as ST Microelectronics USBLC6-2.
R4, R5	Serial termination resistors	Establish a full-speed driver impedance of 28…44 Ohms	A value of 27 Ohms is recommended.
R11	Resistor		10k R is recommended for USB self-powered setup. For bus-powered setup R11 can be ignored.

Table 2: Summary of USB external components

2.3.3 Display Data Channel (DDC)

An I2C compatible DDC interface is available for serial communication. For more information see the *DDC Implementation Application Note* [4].

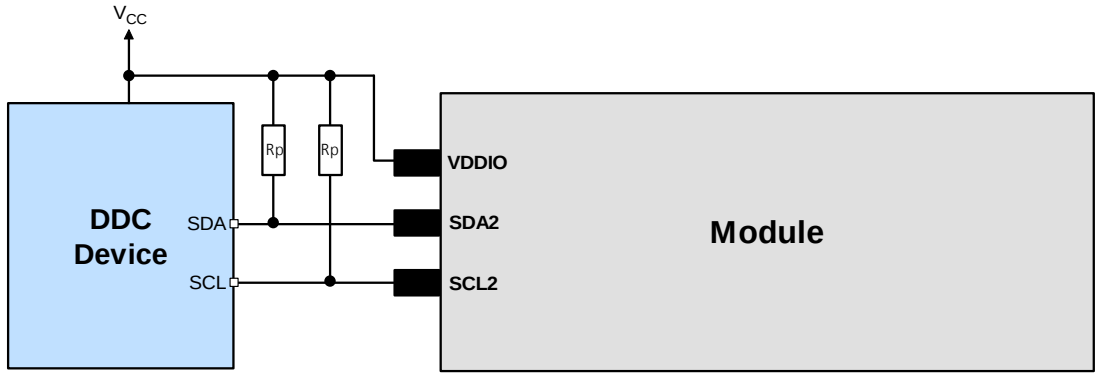


Figure 4: Typical DDC Connection

2.3.4 Synchronous Peripheral Interface (SPI)

An SPI interface is available for serial communication. For more information see the *SPI Implementation Application Note* [5].

☞ No Master Mode: External memory is not supported at this time.

2.4 I/O Pins

2.4.1 RESET_N

As with ANTARIS 4 versions, LEA-5 modules come equipped with a **RESET_N** pin. Driving the signal low at **RESET_N** activates a hardware reset of the system. Unlike LEA-4x modules, **RESET_N** is not an I/O with LEA-5. It is only an input and will not reset external circuitry.

Use components with open drain output (i.e. with buffer or voltage supervisor).

There is an internal pull up resistor of 3k3 to VCC inside the module that requires that the reset circuitry can deliver enough current (e.g. 1mA).

Do not drive **RESET_N** high.

2.4.2 EXTINT0

EXTINT0 is an external interrupt pin with fixed input voltage thresholds independent of VCC (see the *LEA-5 Data Sheet* [3]). Leave open if unused.

2.4.3 AADET_N

AADET_N is an input pin and is used to report whether an external circuit has detected a external antenna or not. Low means antenna has been detected. High means no external antenna has been detected.

See chapter 2.9.5 for an implementation example.

2.4.4 Configuration Pins (CFG_COM0, CFG_COM1, CFG_GPS0)

ROM-based modules provide up to 3 pins (**CFG_COM0, CFG_COM1**, **CFG_GPS0**) for boot-time configuration. These become effective immediately after start-up. Once the module has started, the configuration settings can be modified with UBX configuration messages. The modified settings remain effective until power-down or

reset. If these settings have been stored in battery-backup RAM, then the modified configuration will be retained, as long as the backup battery supply is not interrupted.

Some configuration pins are shared with other functions, e.g. SPI. During start-up, the module reads the state of the configuration pins. Afterwards the other functions can be used.

For more information about settings and messages see the *LEA-5 Data Sheet* [3].

2.5 Design-In

This section provides a Design-In Checklist as well as Reference Schematics for new designs with u-blox 5. For migration of existing ANTARIS®4 product designs to u-blox 5 please refer to *Appendix A*.

Good performance requires a clean and stable power supply with minimal ripple. Care needs to be exercised in selecting a strategy to achieve this. Series resistance in the Vcc supply line can negatively impact performance. For better performance, use an LDO to provide a clean supply at Vcc and consider the following:

- Wide power lines or even power planes are preferred.
- Place LDO near the module.
- Avoid resistive components in the power line (e.g. narrow power lines, coils, resistors, etc.).

Placing a filter or other source of resistance at Vcc can create significantly longer acquisition times.

2.5.1 Schematic Design-In Checklist for LEA-5

Designing-in a LEA-5 GPS/GALILEO receiver is easy especially when a design is based on the reference design in the Hardware Integration Manual. Nonetheless, it pays to do a quick sanity check of the design. This section lists the most important items for a simple design check. The Layout Design-In Checklist also helps to avoid an unnecessary respin of the PCB and helps to achieve the best possible performance.

☞ It is highly recommended to follow the Design-In Checklist when developing any u-blox 5 GPS/GALILEO applications. This can significantly reduce development time and costs.

Have you chosen the optimal module?

LEA-5 modules have been intentionally designed to allow GPS/GALILEO receivers to be optimally tailored to specific applications. Changing between the different variants is easy.

- ❑ Do you need Kick-start performance – Then choose a LEA-5**H**, LEA-5**S**, or LEA-5**Q**.
- ❑ Do you want to be able to upgrade the firmware or to permanently save configuration settings? Then you will have to use a Programmable receiver module: choose a LEA-5H.
- ❑ Do you need USB? All modules based on FW/ROM 5.00 support USB..
- ❑ Do you need Precision Timing – Then choose a LEA-5**T**.

Check Power Supply Requirements and Schematic:

- ❑ Is the power supply within the specified range?
- ❑ Is the voltage **VDDUSB** within the specified range?
- ❑ Compare the peak current consumption of LEA-5 with the specification of your power supply.
- ❑ GPS receivers require a stable power supply, avoid ripple on **VCC** (<50mVpp)

Backup Battery

- ❑ For achieving a minimal Time To First Fix (TTFF), connect a backup battery to **V_BCKP** after power down.

Antenna

- ❑ The total noise figure should be well below 3dB.

- ❑ If a patch antenna is the preferred antenna, choose a patch of at least 15x15mm. For smaller antennas an LNA with a noise figure <2dB is recommended, this can increase sensitivity up to 2dB. To optimize TTFF make use of u-blox' free aiding services AssistNow Online and AssistNow Offline.
- ❑ Make sure the antenna is not placed close to noisy parts of the circuitry. (e.g. micro-controller, display, etc.)
- ❑ For active antennas add a 10R resistor in front of V_ANT4 input for short circuit protection or use the antenna supervisor circuitry.
- ❑ To optimize performance in environments with out-band jamming sources, use an additional SAW filter.

☞ For more information dealing with interference issues see the *GPS Antenna Application Note* [6].

Schematic

- ❑ If required, does your schematic allow using different LEA-5 variants?
- ❑ Don't drive **RESET_N** high!
- ❑ Plan use of 2nd interface (Testpoints on serial port, DDC or USB) for firmware updates or as a service connector.

2.6 LEA-5 Design

For a minimal Design with LEA-5 the following functions and pins need to be considered:

- Connect the Power supply to **VCC.**
- **VDDUSB:** Connect the USB power supply to a LDO before feeding it to **VDDUSB** and **VCC**. Or connect to GND if USB is not used.
- Assure a optimal ground connection to all ground pins of the LEA module
- Connect the antenna to **RF_IN** over a matching 50 Ohm micro strip and define the antenna supply (**V_ANT**)[5] for active antennas (internal or external power supply)
- Choose the required serial communication interface (USART, USB or DDC) and connect the appropriate pins to your application
- If you need Hot- or Warmstart in your application, connect a Backup Battery to **V_BCKP**
- Decide whether **TIMEPULSE** or **RESET_N** options are required in your application and connect the appropriate pins on your module

2.6.1 LEA-5 Passive Antenna Design (LEA-5-H, LEA-5S, LEA-5A, LEA-5T)

This is a minimal setup for a PVT GPS receiver.

[4] Only available with LEA-5-H, LEA-5S, LEA-5A, LEA-5T
[5] Only available with LEA-5-H, LEA-5S, LEA-5A, LEA-5T

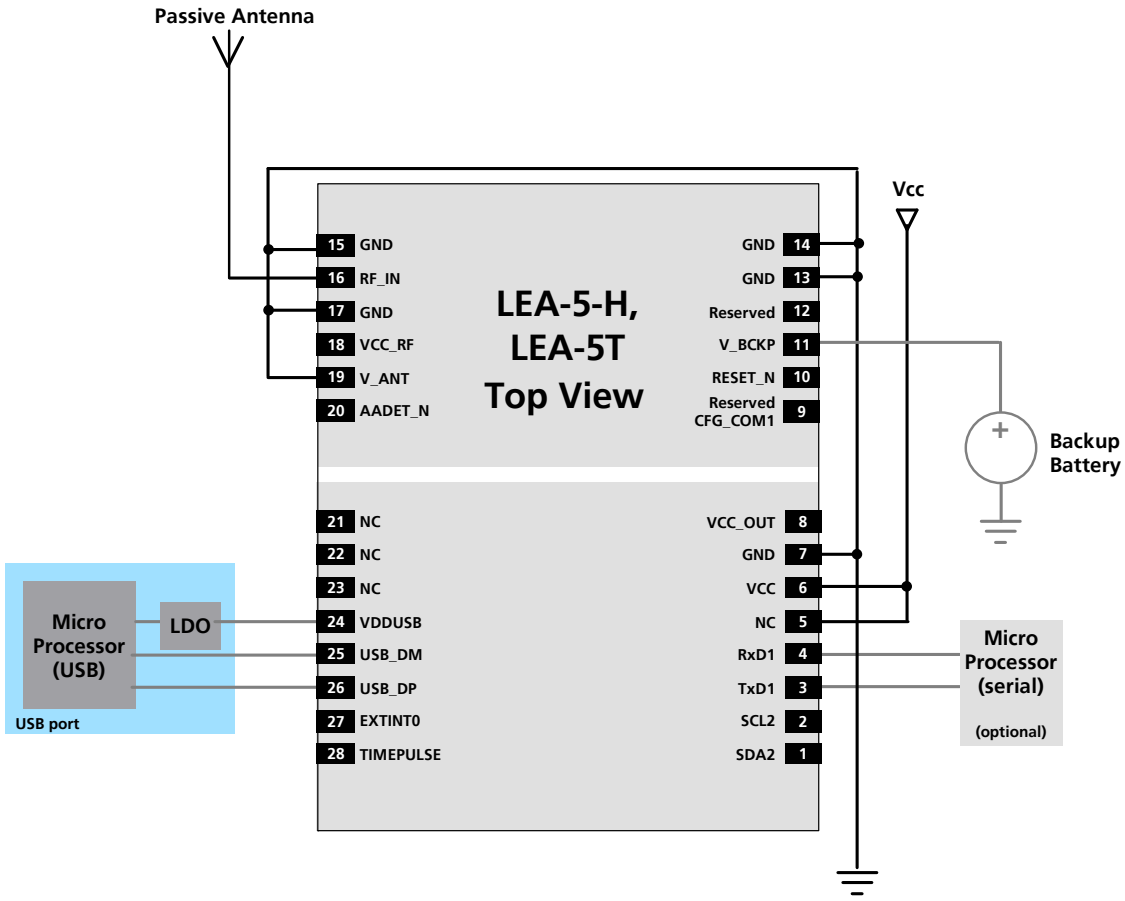


Figure 5: Passive Antenna Design for LEA-5-H, LEA-5T Receivers using USB Port

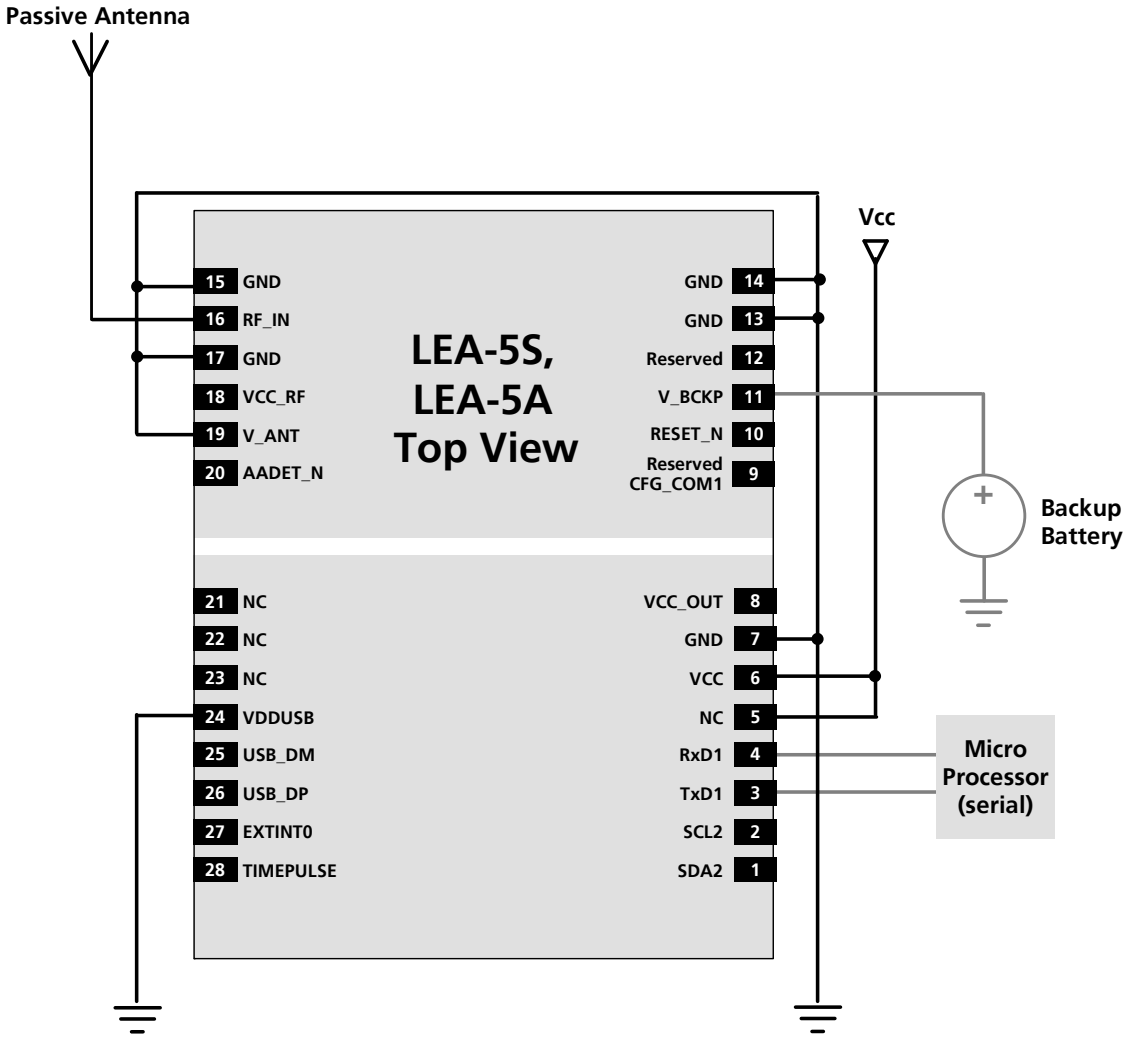


Figure 6: Passive Antenna Design for LEA-5S, LEA-5A Receivers not using USB Port

Function	PIN	I/O	Description	Remarks
Power				
VCC	6	I	Supply Voltage	Provide clean and stable supply.
GND	7, 13-15, 17	I	Ground	Assure a good **GND** connection to all **GND** pins of the module, preferably with a large ground.
VCC_OUT	8	O		Connected to VCC. Leave open if not used.
V_BCKP	11	I	Backup voltage supply	It's recommended to connect a backup battery to **V_BCKP** in order to enable Warm and Hot Start features on the receivers. Otherwise connect to **GND** (or **VCC**).
VDDUSB	24	I	USB Power Supply	To use the USB interface connect this pin to 3.0 – 3.6V derived from VBUS. If no USB serial port used connect to GND.
Antenna				
RF_IN	16	I	GPS/GALILEO signal input from antenna	Use a controlled impedance transmission line of 50 Ohm to connect to RF_IN. Don't supply DC through this pin. Use **V_ANT** pin to supply power.
VCC_RF	18	O	Output Voltage RF section	Can be used to power an external active antenna (**VCC_RF** connected to **V_ANT**). The max power consumption of the Antenna must not exceed the datasheet specification of the module. Leave open if not used.
V_ANT	19	I	Antenna Bias voltage	Connect to **GND** (or leave open) if Passive Antenna is used. If an active Antenna is used, add a 10R resistor in front of **V_ANT** input to the Antenna Bias Voltage or **VCC_RF** for short circuit protection or use the antenna supervisor circuitry.
AADET_N	20	I	Active Antenna Detect	Input pin for optional antenna supervisor circuitry. Leave open if not used.
Serial Port /USB				
TxD1	3	O	Serial Port 1	Serial port output. Leave open if not used.
RxD1	4	I	Serial Port 1	Serial port input with internal pull-up resistor to VCC. Leave open if not used. Don't use external pull up resistor.
USB_DM	25	I/O	USB I/O line	USB2.0 bidirectional communication pin. Leave open if unused. Implementation see Section 2.3.2.
USB_DP	26			
System				
RESET_N	10	I	Hardware Reset (Active Low)	Leave open if not used. Do not drive high.
TIMEPULSE	28	O	Timepulse Signal	Configurable Timepulse signal (one pulse per second by default). Leave open if not used.
EXTINT0	27	I	External Interrupt	External Interrupt Pin. Internal pull-up resistor to **VCC**. Leave open if not used.
CFG_COM1/ Reserved	9	I	Configuration Pin/ Reserved	LEA-5S, LEA-5A: Leave open for default configuration. LEA-5H, LEA-5T: Reserved
SDA2	1	I/O	DDC Pins	DDC Data. Leave open if not used.
SCL2	2			DDC Clock. Leave open if not used.
Reserved	12	I		Leave open, do not drive low.
NC	5			Can be left open, but **connection to VCC is recommended** for compatibility reasons. I/O voltage is always VCC.
NC	21-22		Not Connect	Leave open
NC	23		Not Connect	Leave open

Table 3: Pinout LEA-5-H, LEA-5S, LEA-5A, LEA-5T

2.6.2 Passive Antenna Design (LEA-5-Q, LEA-5M)

This is a minimal setup for a PVT GPS receiver.

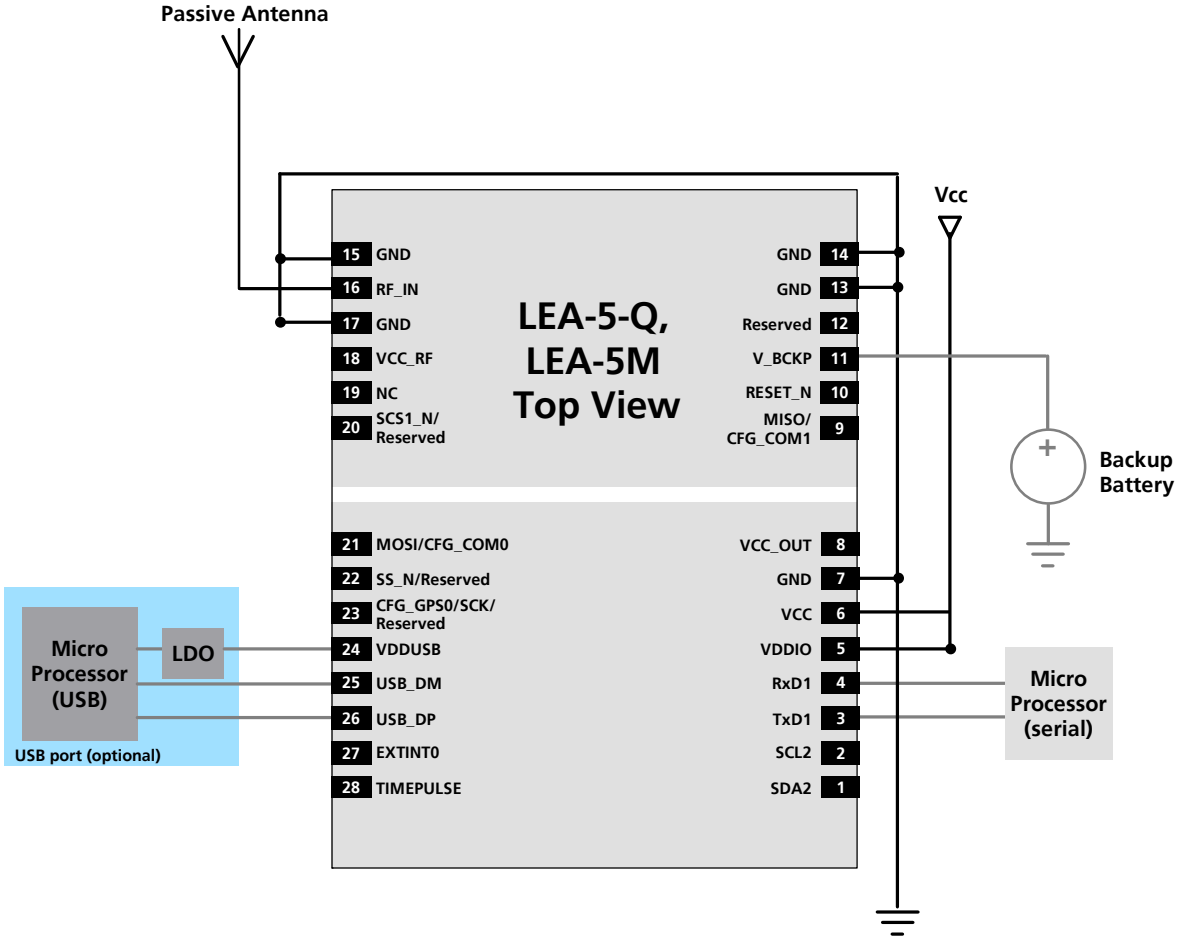


Figure 7: Pinout LEA-5-Q, LEA-5M

☞ The above design is for the USB in BUS-powered mode. For Self-powered mode pin 21 (CFG_COM0) must be connected to GND. In this case the NMEA baud rate on UART1 of 38400. For more information see the *LEA-5 Data Sheet* [3].

☞ For passive antenna designs use an LNA to increase sensitivity up to 2dB.

Function	PIN	I/O	Description	Remarks
Power				
VCC	6	I	Supply Voltage	Provide clean and stable supply.
GND	7, 13-15, 17	I	Ground	Assure a good **GND** connection to all **GND** pins of the module, preferably with a large ground plane.
VCC_OUT	8	O		Connected to VCC. Leave open if not used.
V_BCKP	11	I	Backup voltage supply	It's recommended to connect a backup battery to **V_BCKP** in order to enable Warm and Hot Start features on the receivers. Otherwise connect to **GND** (or VCC).
VDDUSB	24	I	USB Power Supply	To use the USB interface connect this pin to 3.0-3.6V derived from VBUS. If no USB serial port used connect to GND.
VDDIO	5	I	I/O Voltage	Defines the I/O voltage. Do not leave open.
Antenna				
RF_IN	16	I	GPS/GALILEO signal input from antenna	Use a controlled impedance transmission line of 50 Ohm to connect to RF_IN. Antenna bias voltage for active antennas is not provided on the **RF_IN** pin. If an active Antenna is used an external voltage is required (see *Section 2.9.3)*.
VCC_RF	18	O	Output Voltage RF section	Leave open
Serial Port /USB				
TxD1	3	O	Serial Port 1	Serial port output. Leave open if not used.
RxD1	4	I	Serial Port 1	Serial port input with internal pull-up resistor to VCC. Leave open if not used. Don't use an external pull up resistor.
USB_DM	25	I/O	USB I/O line	USB2.0 bidirectional communication pin. Leave open if unused. Implementation see Section 2.3.2.
USB_DP	26			
System				
RESET_N	10	I	Hardware Reset (Active Low)	Leave open if not used. Do not drive high.
TIMEPULSE	28	O	Timepulse Signal	Configurable Timepulse signal (one pulse per second by default). Leave open if not used.
EXTINT0	27	I	External Interrupt	External Interrupt Pin. Internal pull-up resistor to **VCC**. Leave open if not used.
SDA2	1	I/O	DDC Pins	DDC Data. Leave open, if not used.
SCL2	2			DDC Clock. Leave open, if not used.
Reserved	12	I		Leave open, do not drive low.
NC	19		Not Connected	Leave open.
SCS1_N/ Reserved	20	O	SPI	LEA-5Q: SPI Chip Select. Leave open if not used. LEA-5M: Leave open.
MISO/ CFG_COM1	9	I/O	SPI Configuration Pin	LEA-5Q: SPI MISO. Leave open, if not used. LEA-5Q/LEA-5M: Leave open for default configuration.
MOSI/ CFG_COM0	21	I/O	SPI Configuration Pin	LEA-5Q: SPI MOSI. Leave open, if not used. LEA-5Q/LEA-5M: Leave open for default configuration.
SS_N/ Reserved	22	I	SPI Reserved	LEA-5Q: SPI Slave Select. Leave open, if not used. LEA-5M: Leave open.
SCK/CFG_GPS/ Reserved	23	I/O	SPI/Power Mode	LEA-5Q: SPI Clock / Power Mode Configuration Pin. Leave open, if not used. LEA-5M: Leave open.

Table 4: Pinout LEA-5-Q, LEA-5M

2.7 Layout Design-In Checklist

Follow this checklist for the Layout design to get an optimal GPS performance.

Layout optimizations (*Section 2.8*)

- ❑ Is the GPS module placed according to the recommendation in Section 2.8.3?
- ❑ Has the Grounding concept been followed (see Section 2.8.4)?
- ❑ Has the micro strip been kept as short as possible?
- ❑ Add a ground plane underneath the GPS module to reduce interference.
- ❑ For improved shielding, add as many vias as possible around the micro strip, around the serial communication lines, underneath the GPS module etc.
- ❑ Have ESD protection measures been included (see Section 2.10)?

Calculation of the micro strip (*Section 2.8.5*)

- ❑ The micro strip must be 50 Ohms and be routed in a section of the PCB where minimal interference from noise sources can be expected.
- ❑ In case of a multi-layer PCB, use the thickness of the dielectric between the signal and the 1st GND layer (typically the 2nd layer) for the micro strip calculation.
- ❑ If the distance between the micro strip and the adjacent GND area (on the same layer) does not exceed 5 times the track width of the micro strip, use the "Coplanar Waveguide" model in AppCad to calculate the micro strip and not the "micro strip" model.

2.8 Layout

This section provides important information for designing a reliable and sensitive GPS/GALILEO system.

GPS signals at the surface of the Earth are about 15dB below the thermal noise floor. Signal loss at the antenna and the RF connection must be minimized as much as possible. When defining a GPS receiver layout, the placement of the antenna with respect to the receiver, as well as grounding, shielding and jamming from other digital devices are crucial issues and need to be considered very carefully.

2.8.1 Footprint

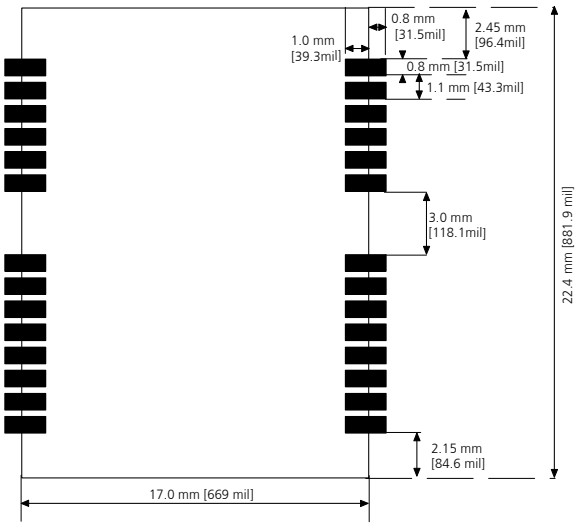


Figure 8: Recommended footprint

2.8.2 Paste Mask

Figure 9 shows the recommended positioning of the Paste Mask, the Copper and Solder masks. These are recommendations only and not specifications. Note that the Copper and Solder masks have the same size and position.

To improve the wetting of the half vias, reduce the amount of solder paste under the module and increase the volume outside of the module by defining the dimensions of the paste mask to form a T-shape (or equivalent) extending beyond the Copper mask as shown in Figure 9. The solder paste should have a total thickness of 175 to 200 µm.

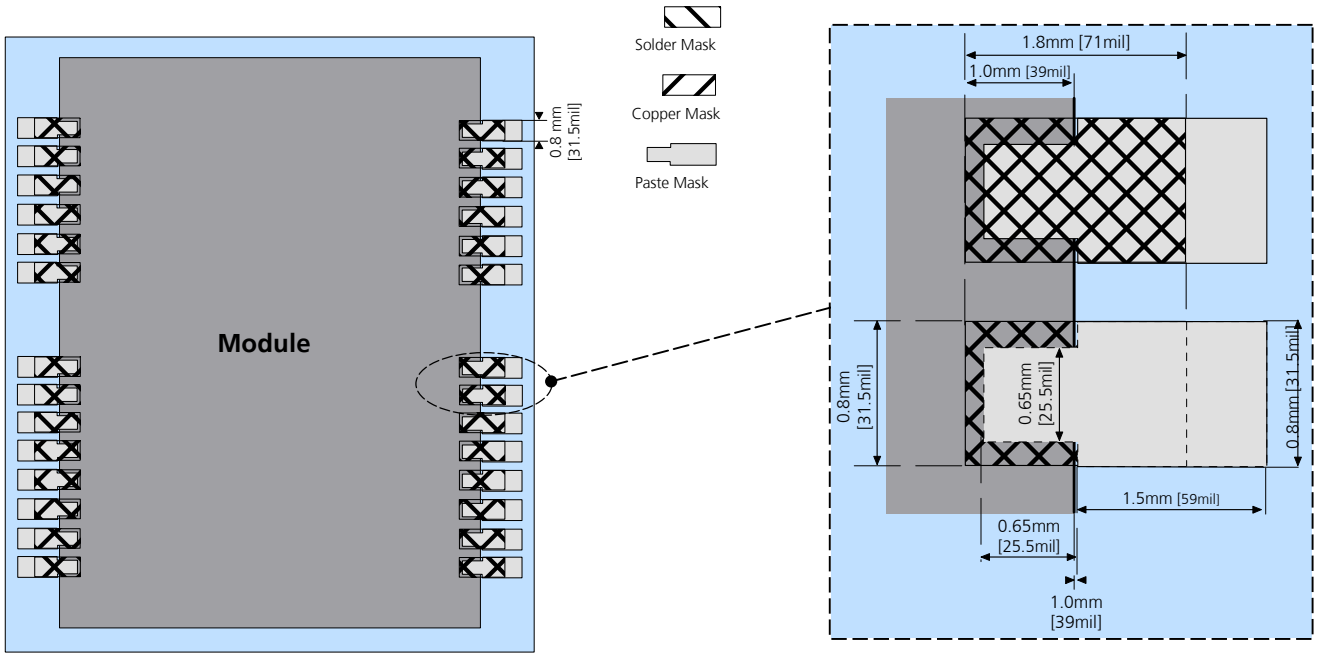


Figure 9: Recommendations for copper, solder and paste masks with enlargement

☞ The paste mask outline needs to be considered when defining the minimal distance to the next component.

☞ The exact geometry, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) of the customer.

2.8.3 Placement

A very important factor in achieving maximum GPS and GALILEO performance is the placement of the receiver on the PCB. The connection to the antenna must be as short as possible to avoid jamming into the very sensitive RF section.

Make sure that RF critical circuits are clearly separated from any other digital circuits on the system board. To achieve this, position the receiver digital part towards your digital section of the system PCB. Care must also be exercised with placing the receiver in proximity to circuitry that can emit heat. The RF part of the receiver is very sensitive to temperature and sudden changes can have an adverse impact on performance.

⚠ **The RF part of the receiver is a temperature sensitive component. Avoid high temperature drift and air vents near the receiver.**

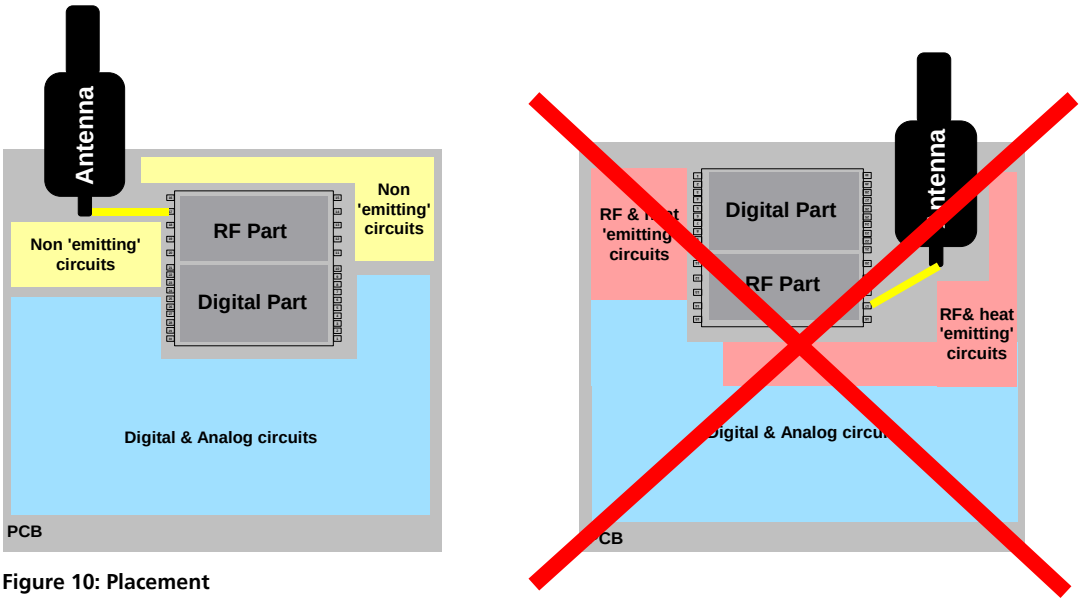


Figure 10: Placement

2.8.4 Antenna Connection and Grounding Plane Design

u-blox 5 modules can be connected to passive patch or active antennas. The RF connection is on the PCB and connects the **RF_IN** pin with the antenna feed point or the signal pin of the connector, respectively. *Figure 11* illustrates connection to a typical five-pin RF connector. One can see the improved shielding for digital lines as discussed in the *GPS Antenna Application Note* [6]. Depending on the actual size of the ground area, additional vias should be placed in the outer region. In particular, the edges of the ground area should be terminated with a dense line of vias.

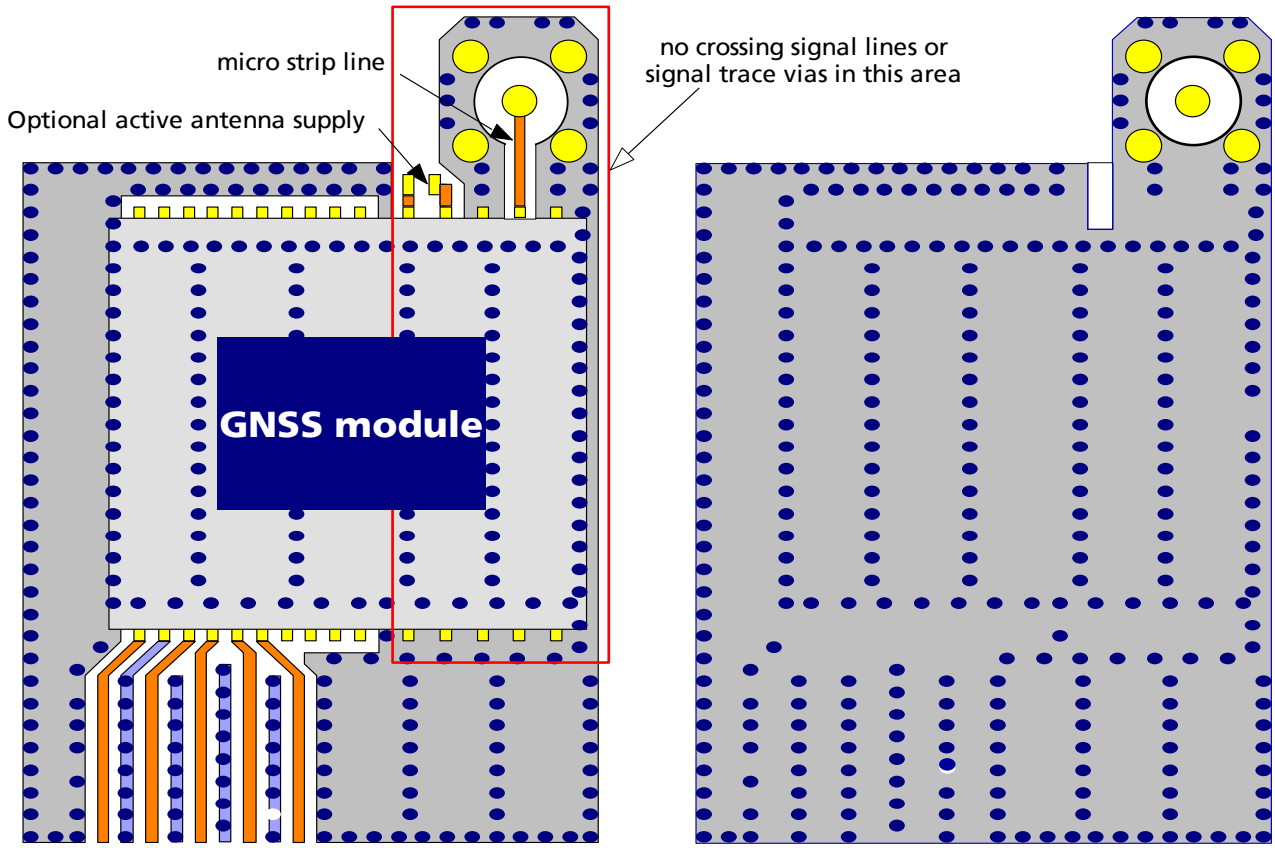


Figure 11: Recommended layout

As seen in *Figure 11*, an isolated ground area is created around and below the RF connection. This part of the circuit MUST be kept as far from potential noise sources as possible. Make certain that no signal lines cross, and that no signal trace vias appear at the PCB surface within the area of the red rectangle. The ground plane should also be free of digital supply return currents in this area. On a multi layer board, the whole layer stack below the RF connection should be kept free of digital lines. This is because even solid ground planes provide only limited isolation.

The impedance of the antenna connection has to match the 50 Ohm impedance of the receiver. To achieve an impedance of 50 Ohms, the width W of the micro strip has to be chosen depending on the dielectric thickness H, the dielectric constant ε_r of the dielectric material of the PCB and on the build-up of the PCB (see *Section 2.8.5*). *Figure 12* shows two different builds: A 2 Layer PCB and a 4 Layer PCB. The reference ground plane is in both designs on layer 2 (red). Therefore the effective thickness of the dielectric is different.

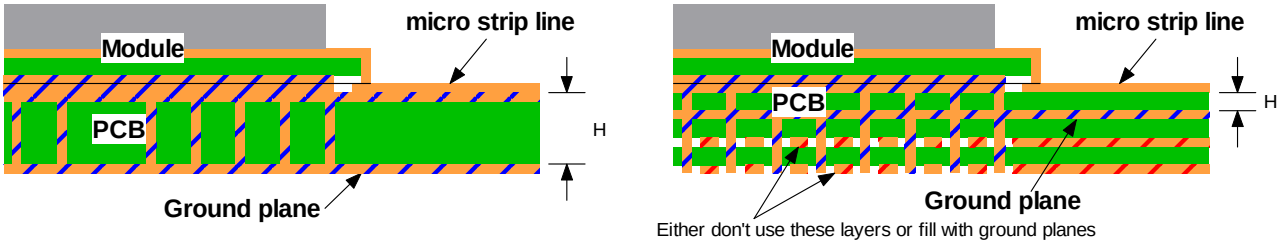
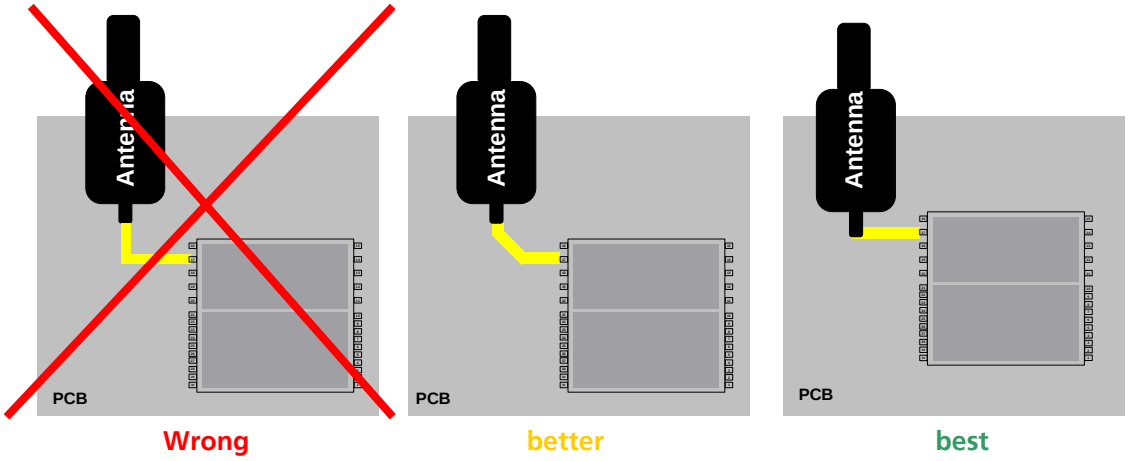


Figure 12: PCB build-up for Micro strip line. Left: 2-layer PCB, right: 4-layer PCB

General design recommendations:

- The length of the micro strip line should be kept as short as possible. Lengths over 2.5 cm (1 inch) should be avoided on standard PCB material and without additional shielding.
- Distance between micro strip line and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF connection close to digital sections of the design should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.



- Routing of the RF-connection underneath the receiver should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small (some 100 µm) and has huge tolerances (up to 100%). Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.
- In order to avoid reliability hazards, the area on the PCB under the receiver should be entirely covered with solder mask. Vias should not be open.

2.8.5 Antenna Micro Strip

There are many ways to design wave-guides on printed circuit boards. Common to all is that calculation of the electrical parameters is not straightforward. Freeware tools like AppCAD from Agilent or TXLine from Applied Wave Research, Inc. are of great help. They can be downloaded from *www.agilent.com* and *www.mwoffice.com*.

The micro strip is the most common configuration for printed circuit boards. The basic configuration is shown in *Figure 13* and *Figure 14*. As a rule of thumb, for a FR-4 material the width of the conductor is roughly double the thickness of the dielectric to achieve 50 Ohms line impedance.

For the correct calculation of the micro strip impedance, one does not only need to consider the distance between the top and the first inner layer but also the distance between the micro strip and the adjacent GND plane on the same layer

☞ Use the Coplanar Waveguide model for the calculation of the micro strip.

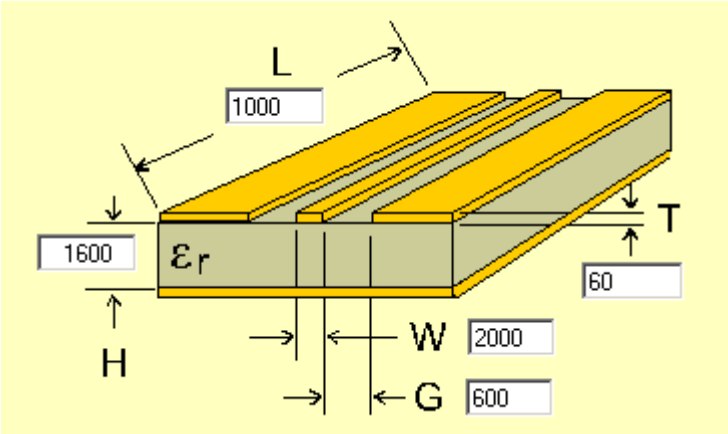


Figure 13: Micro strip on a 2-layer board (Agilent AppCAD Coplanar Waveguide)

Figure 13 shows an example of a 2-layer FR4 board of 1.6 mm thickness and a 35µm (1 once) copper cladding. The thickness of the micro strip is comprised of the cladding (35µm) plus the plated copper (typically 25µm). *Figure 14* depicts an example of a multi layer FR4 board with 18µm (½ once) cladding and 180µ dielectric between layer 1 and 2.

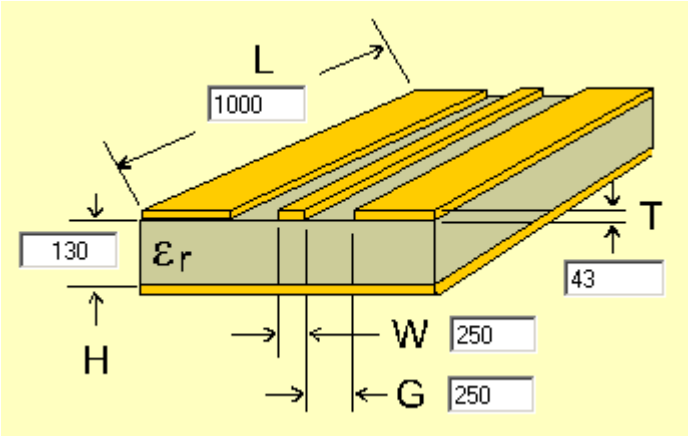


Figure 14: Micro strip on a multi layer board (Agilent AppCAD Coplanar Waveguide)

2.9 Antenna and Antenna Supervisor

u-blox 5 modules receive L1 band signals from GPS and GALILEO satellites at a nominal frequency of 1575.42 MHz. The RF signal is connected to the **RF_IN** pin.

u-blox 5 modules can be connected to passive or active antennas.

☞ For u-blox 5 receivers, the total preamplifier gain (minus cable and interconnect losses) must not exceed 50 dB. Total noise figure should be below 3 dB.

The u-blox 5 Technology supports either a short circuit protection of the active antenna or an active antenna supervisor circuit (open and short circuit detection). For further information refer to *Section 2.9.2).*

2.9.1 Passive Antenna

A design using a passive antenna requires more attention regarding the layout of the RF section. Typically a passive antenna is located near electronic components; therefore care should be taken to reduce electrical 'noise' that may interfere with the antenna performance. Passive antennas do not require a DC bias voltage and can be directly connected to the RF input pin **RF_IN**. Sometimes, they may also need a passive matching network to match the impedance to 50 Ohms.

☞ Some passive antenna designs present a DC short to the RF input, when connected. If a system is designed with antenna bias supply AND there is a chance of a passive antenna being connected to the design, consider a short circuit protection.

☞ All u-blox 5 receivers have a built-in LNA required for passive antennas.

2.9.2 Active Antenna (LEA-5H, LEA-5S, LEA-5A, LEA-5T)

Active antennas have an integrated low-noise amplifier. They can be directly connected to **RF_IN**. If an active antenna is connected to **RF_IN**, the integrated low-noise amplifier of the antenna needs to be supplied with the correct voltage through pin **V_ANT** or an external inductor. Usually, the supply voltage is fed to the antenna through the coaxial RF cable. Active antennas require a power supply that will contribute to the total GPS system power consumption budget with additional 5 to 20 mA typically. Inside the antenna, the DC component on the inner conductor will be separated from the RF signal and routed to the supply pin of the LNA (see Figure 15).

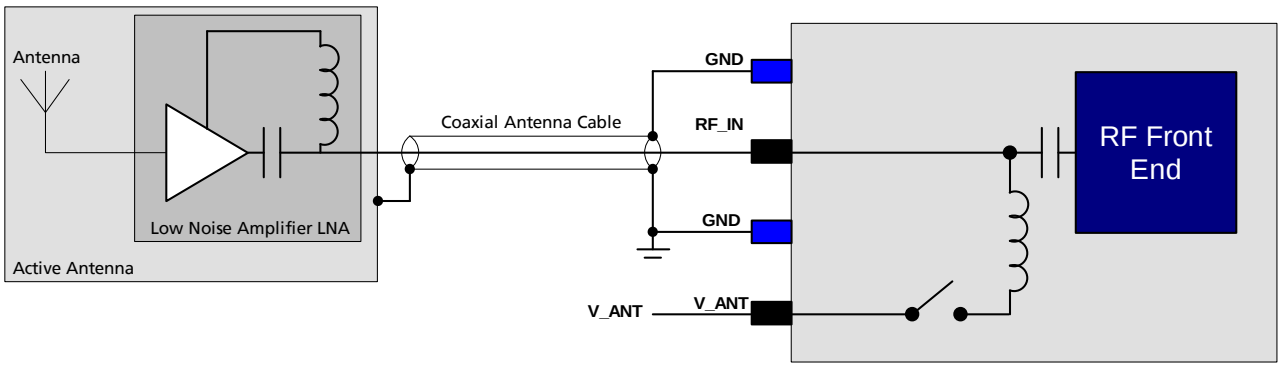


Figure 15: Active antenna biasing

Generally an active antenna is easier to integrate into a system design, as it is less sensitive to jamming compared to a passive antenna. But an active antenna must also be placed far from any noise sources to have good performance.

Antennas should only be connected to the receiver when the receiver is not powered. Do not connect or disconnect the Antenna when the u-blox 5 receiver is running as the receiver calibrates the noise floor on power-up. Connecting the antenna after power-up can result in prolonged acquisition time.

Never feed supply voltage into RF_IN. Always feed via V_ANT or an external inductor .

☞ To test GPS/GALILEO signal reacquisition, it is recommended to physically block the signal to the antenna, rather than disconnecting and reconnecting the receiver.

2.9.3 Active Antenna (LEA-5Q, LEA-5M)

LEA-5-Q and LEA-5M modules do not provide the antenna bias voltage for active antennas on the **RF_IN** pin. It is therefore necessary to provide this voltage outside the module via an inductor as indicated in Figure 16. u-blox recommends using an inductor from Murata (LQG15HS27NJ02). Alternative parts can be used if the inductor's resonant frequency matches the GPS frequency of 1575.4MHz.

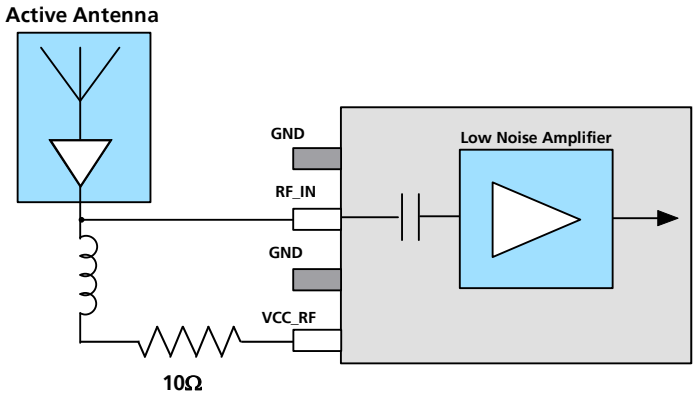


Figure 16: Recommended wiring for active antennas

For optimal performance, it is important to place the inductor as close to the microstrip as possible. Figure 15 illustrates the recommended layout and how it should not be done.

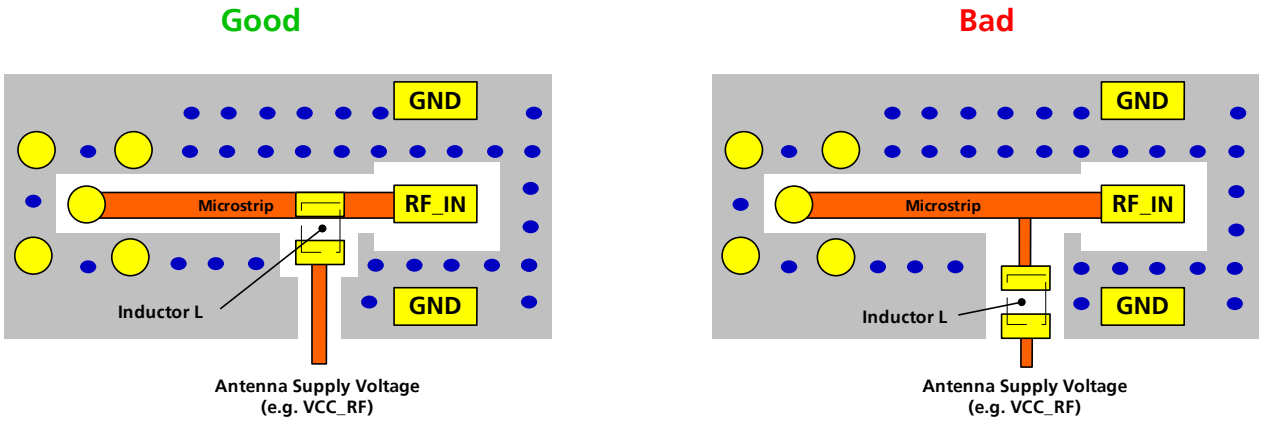


Figure 17: Recommended layout for connecting the antenna bias voltage for LEA-5Q and LEA-5M

2.9.4 Active Antenna Bias Power (LEA-5H, LEA-5S, LEA-5A, LEA-5T)

There are two ways to supply the bias voltage to pin **V_ANT**. It can be supplied externally (please consider the datasheet specification) or internally. For Internal supply, the **VCC_RF** output must be connected to **V_ANT** to supply the antenna with a filtered supply voltage. However, the voltage specification of the antenna has to match the actual supply voltage of the u-blox 5 Receiver (e.g. 3.0 V).

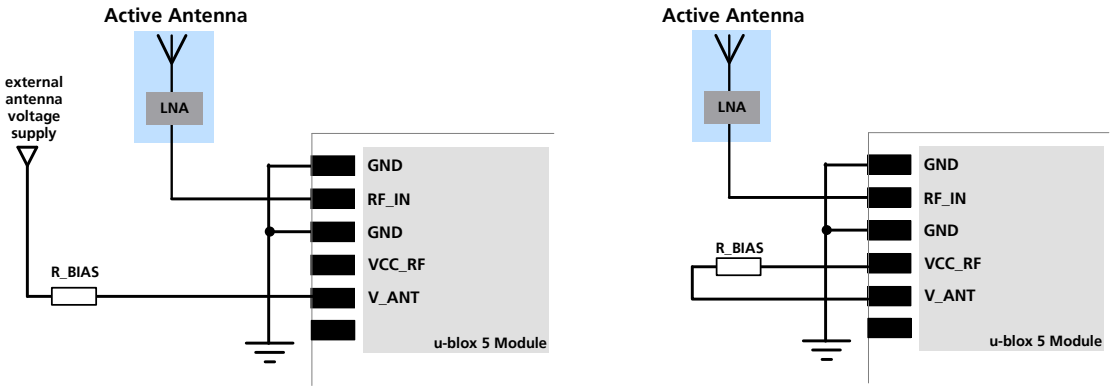


Figure 18: Supplying Antenna bias voltage

Since the bias voltage is fed into the most sensitive part of the receiver, i.e. the RF input, this supply should be virtually free of noise. Usually, low frequency noise is less critical than digital noise with spurious frequencies with harmonics up to the GPS/GALILEO band of 1.575 GHz. Therefore, it is not recommended to use digital supply nets to feed pin **V_ANT**.

An internal switch (under control of the u-blox 5 software) can shutdown the supply to the external antenna whenever it is not needed. This feature helps to reduce power consumption.

2.9.4.1 Short Circuit Protection

If a reasonably dimensioned series resistor **R_BIAS** is placed in front of pin **V_ANT**, a short circuit situation can be detected by the baseband processor. If such a situation is detected, the baseband processor will shut down supply to the antenna. The receiver is by default configured to attempt to reestablish antenna power supply periodically.

☞ To configure the antenna supervisor use the UBX-CFG-ANT message. For further information refer to the *u-blox 5 Protocol Specification [1].*

References	Value	Tolerance	Description	Manufacturer
R_BIAS	10 Ω	± 10%	Resistor, min 0.250 W	

Table 5: Short circuit protection, bill of material

⚠ **Short circuits on the antenna input without limitation of the current can result in permanent damage to the receiver! Therefore, it's recommended to implement an R_BIAS in all risk applications, such as situations where the antenna can be disconnected by the end-user or that have long antenna cables.**

☞ An additional R_BIAS is not required when using a short and open active antenna supervisor circuitry as defined in *Section 2.9.5.1*, as the R_BIAS is equal to R2.

2.9.5 Active Antenna Supervisor (LEA-5H, LEA-5S, LEA-5A, LEA-5T)

u-blox 5 Technology provides the means to implement an active antenna supervisor with a minimal number of parts. The antenna supervisor is highly configurable to suit various different applications.

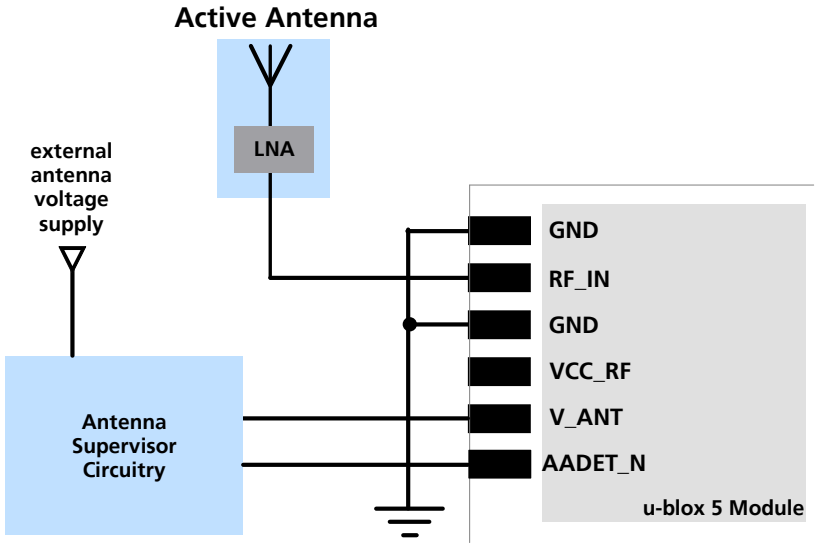


Figure 19: External antenna power supply with full antenna supervisor

2.9.5.1 Short and Open Circuit Active Antenna Supervisor

The Antenna Supervisor can be configured by a serial port message (using only UBX binary message).

When enabled the active antenna supervisor produces serial port messages (status reporting in NMEA and/or UBX binary protocol) which indicates all changes of the antenna circuitry (**disabled** antenna supervisor, antenna circuitry **ok**, **short** circuit, **open** circuit) and shuts the antenna supply down if required.

The active antenna supervisor provides the means to check the active antenna for open and short circuits and to shut the antenna supply off, if a short circuit is detected.

The following state diagram applies. If an antenna is connected, the initial state after power-up is "Active Antenna OK".

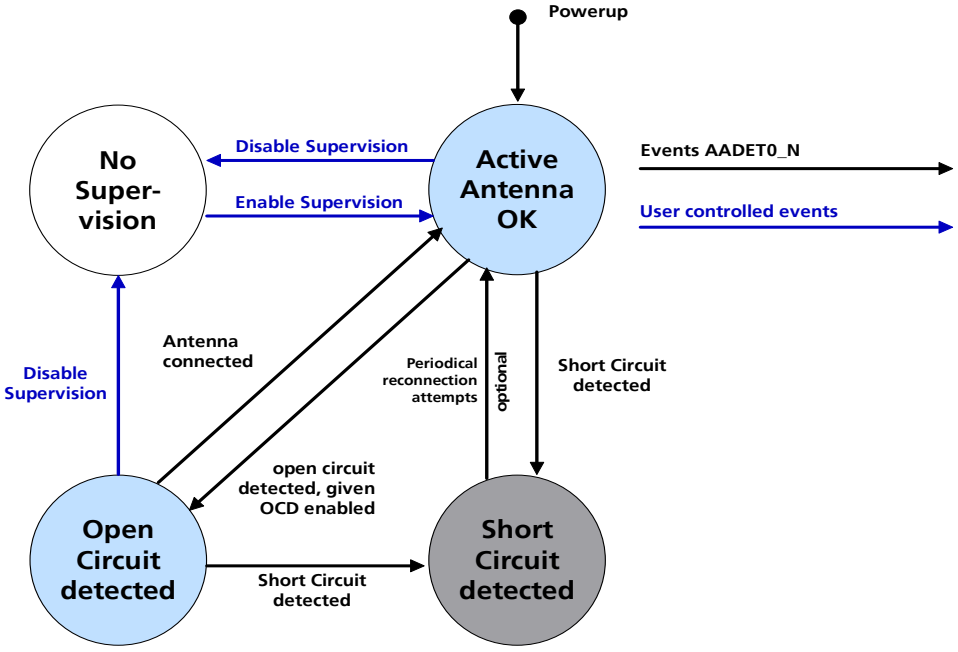


Figure 20: State Diagram of Active Antenna Supervisor

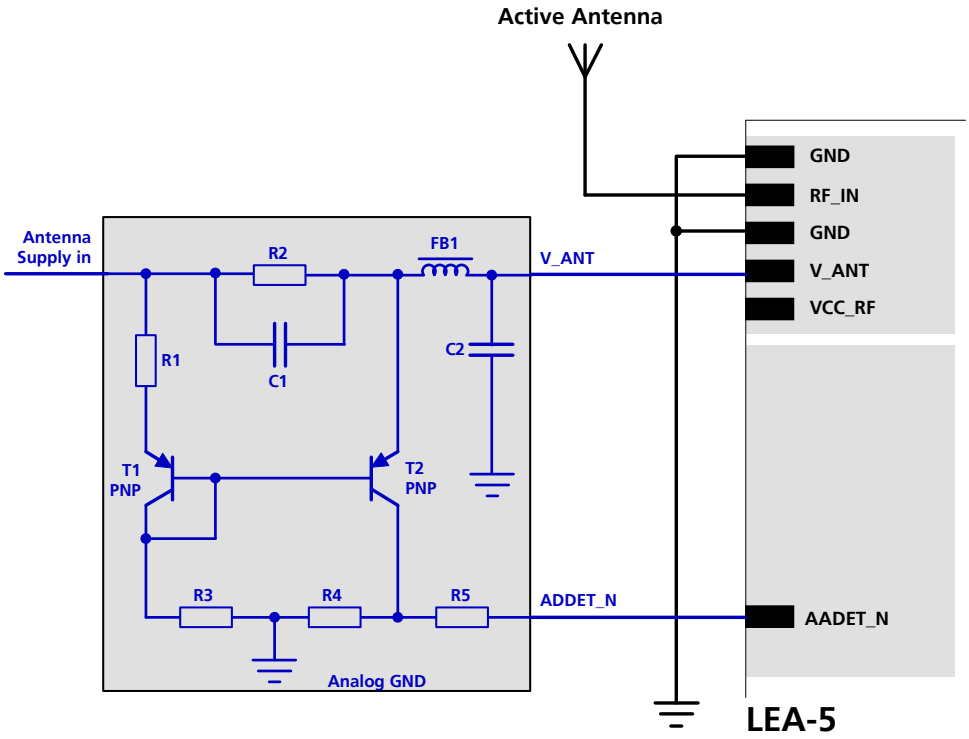


Figure 21: Schematic of open circuit detection

References	Value	Tolerance	Description	Remarks
C1	2.2 µF	± 10%	Capacitor, X7R, min 10 V	
C2	100 nF	± 10%	Capacitor, X7R, min 10 V	
FB1	600 Ω		Ferrite Bead	e.g. Murata BLM18HD601SN1
R1	15 Ω	± 10%	Resistor, min 0.063 W	
R2	10 Ω	± 10%	Resistor, min 0.250 W	
R3, R4	10 kΩ	± 10%	Resistor, min 0.063 W	
R5	33 kΩ	± 10%	Resistor, min 0.063 W	
T1, T2			PNP Transistor BC856B	e.g. Philips Semiconductors[6]

Table 6: Active Antenna Supervisor, bill of material

Firmware supports an active antenna supervisor circuit, which is connected to the pin **AADET_N**. An example of an open circuit detection circuit is shown in Figure 21. High on **AADET_N** means that an external antenna is not connected.

Short Circuit Detection (SCD)

A short circuit in the active antenna pulls **V_ANT** to ground. This is detected inside the u-blox 5 module and the antenna supply voltage will be immediately shut down.

☞ Antenna short detection (SCD) and control is enabled by default.

[6] Transistors from other suppliers with comparable electrical characteristics may be used.

Open Circuit Detection (OCD)

The open circuit detection circuit uses the current flow to detect an open circuit in the antenna. The threshold current is 2.5mA (at 2.7V) and 5.1mA (at 5.5V) respectively (applies to resistor values according to Figure 21 and at room temperature).

If the current through T2 is large, the voltage drop through R4 and therefore AADET_N will be high, indicating an open connection. On the other hand, if the current is small, AADET_N will be low.

Status Reporting

At startup and on every change of the antenna supervisor configuration the u-blox 5 GPS/GALILEO module will output a NMEA ($GPTXT) or UBX (INF-NOTICE) message with the internal status of the antenna supervisor (disabled, short detection only, enabled).

None, one or several of the strings below are part of this message to inform about the status of the active antenna supervisor circuitry (e.g. "ANTSUPERV= AC SD OD PdoS").

Abbreviation	Description
AC	Antenna Control (e.g. the antenna will be switched on/ off controlled by the GPS receiver)
SD	Short Circuit Detection Enabled
OD	Open Circuit Detection Enabled
PdoS	Power Down on short

Table 7: Active Antenna Supervisor Message on startup (UBX binary protocol)

☞ To activate the antenna supervisor use the UBX-CFG-ANT message. For further information refer to the *u-blox 5 Protocol Specifications [1].*

Similar to the antenna supervisor configuration, the status of the antenna supervisor will be reported in a NMEA ($GPTXT) or UBX (INF-NOTICE) message at start-up and on every change.

Message	Description
ANTSTATUS=DONTKNOW	Active antenna supervisor is not configured and deactivated.
ANTSTATUS=OK	Active antenna connected and powered
ANTSTATUS=SHORT	Antenna short
ANTSTATUS=OPEN	Antenna not connected or antenna defective

Table 8: Active Antenna Supervisor Message on startup (NMEA protocol)

☞ The open circuit supervisor circuitry has a quiescent current of approximately 2mA. This current may be reduced with an advanced circuitry, which fulfils the same function as the u-blox suggested circuitry.

2.10 ESD Protection Measures

GPS receivers are Electrostatic Sensitive Devices (ESD). Special precautions are required when handling (see Section 3.4).

2.10.1 ESD Precautions for USB

In addition to handling precautions, design measures can protect the GPS device from potential damage caused by Electrostatic surges. With USB interfaces, protection devices (e.g. ST Microelectronics USBLC6-2) can introduce ESD resistance into the design. Carefully considering the layout is very important. ESD protection devices should be placed as close as possible to the sources of possible ESD disturbance (e.g. connectors). Figure 22 shows an example of using ESD protection with a USB connection. The data lines between I/O pins, from VDD_USB to VBUS pin and from GND plane to GND pin should be as short as possible.

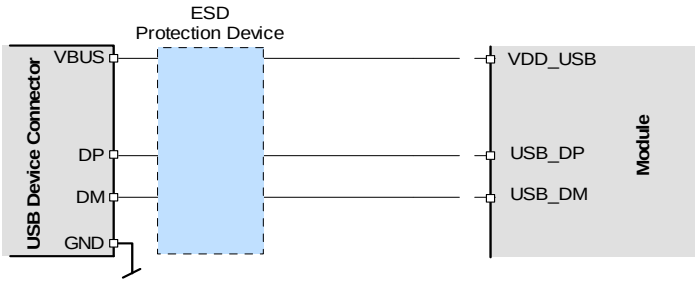


Figure 22: ESD protection for USB designs

2.10.2 ESD Precautions for Antennas

Antennas are an area of particular ESD sensitivity for GPS receivers. For improved resistance to external transient voltage spikes ESD protection circuits can be used. For passive antennas introduce a coil between the module and the patch (see Figure 23). By using a low capacitance ESD protection diode in an active antenna design it is possible to achieve ESD protection IEC-61000-2-4 Level 1 (see Figure 24).

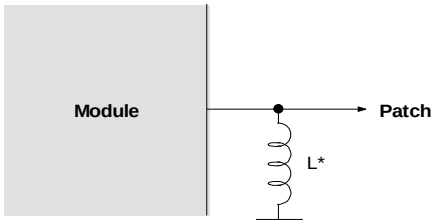


Figure 23: ESD Protection Circuit for Passive Antenna

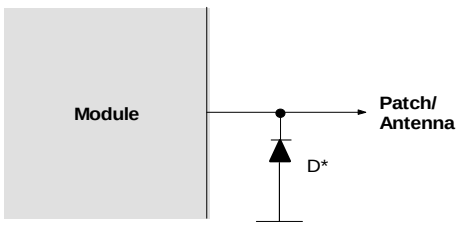


Figure 24: ESD Protection Circuit for Active Antenna

Component	Example
L*	IND MURATA LQG15H 0402 27N 5% 300MA
D*	ESD9L5.0ST5G Vant >3.3V ESD9R3.3ST5G ESD9L3.3ST5G

Table 9: Protection Circuit Components

3 Product Handling

☞ All LEA-5 modules are RoHS compliant (lead-free).

3.1 Packaging

LEA-5 modules are delivered as hermetically sealed, reeled tapes in order to enable efficient production, production lot set-up and tear-down.

Figure 25: Reeled u-blox 5 Modules

3.1.1 Reels

LEA-5 modules for GPS and GALILEO are deliverable in quantities of 250pcs on a reel. The dimensions of the reel are shown in *Figure 26*.

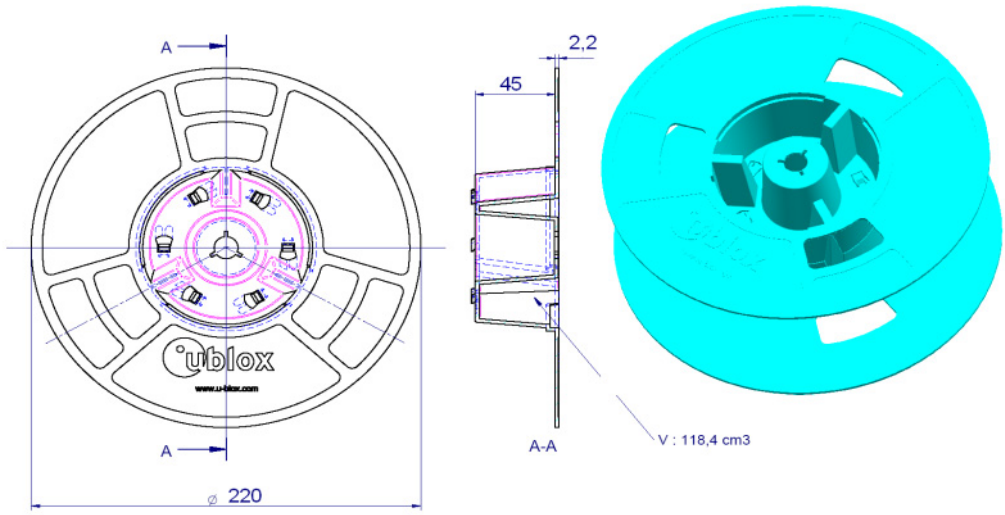


Figure 26: Dimension of reel for 250 pieces (dimensions unless otherwise specified in mm)

3.1.2 Tapes

The dimensions and orientations of the tapes for LEA 5 modules are specified in Figure 27.

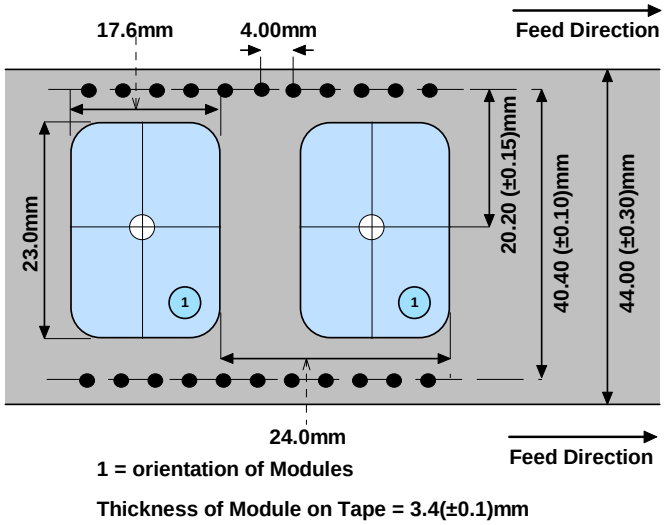


Figure 27: Dimensions and orientation for LEA- 5 modules on tape

3.2 Shipment, Storage and Handling

3.2.1 Handling

u-blox 5 modules are designed and packaged to be processed in an automatic assembly line, and are shipped in Tape-and-Reel.

These components contain highly sensitive electronic circuitry. Handling the LEA-5 modules without proper ESD protection may destroy or damage them permanently.

According to JEDEC ISP, LEA-5 modules are moisture sensitive devices. Appropriate handling instructions and precautions are summarized in *Sections 3.2.2* to *3.2.5.* Read them carefully to prevent permanent damages due to moisture intake.

3.2.2 Shipment

The LEA-5 modules are delivered on Tape-and-Reels in a hermetically sealed package ("dry bag") to prevent moisture intake and protect against electrostatic discharge. For protection from physical damage, the reels are individually packed in cartons.

The dry bag provides a JEDEC compliant MSD label (Moisture Sensitive Devices) describing the handling requirements to prevent humidity intake.

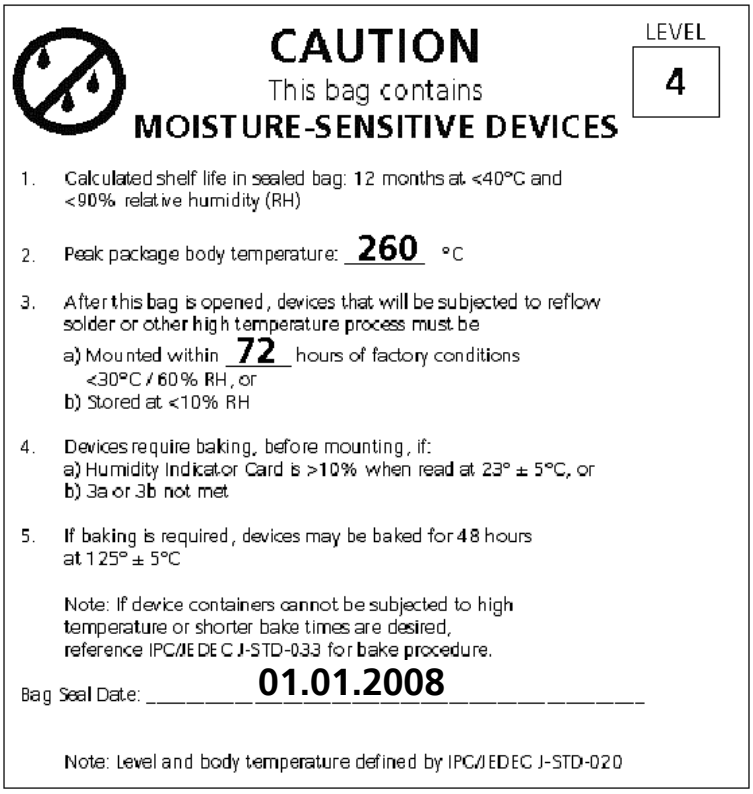


Figure 28: Applicable MSD Label (See *Section 3.1* for baking instructions)

3.2.3 Storage

Shelf life in sealed bag is 12 months at <40°C and <90% relative humidity.

3.2.4 Handling

A humidity indicator card and a desiccant bag to absorb humidity are enclosed in the sealed package. The parts are shipped on tape-and-reel in a hermetically sealed package. If no moisture has been absorbed, the three fields in the humidity indicator card indicate blue color.

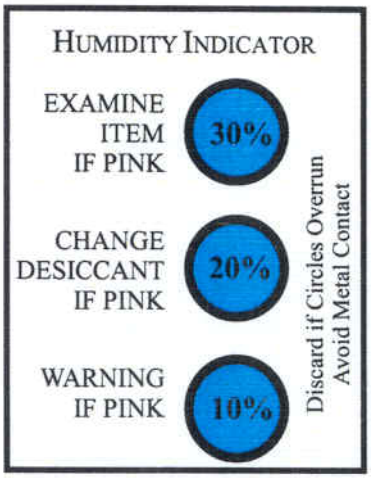


Figure 29: Humidity Indicator Card, good condition

3.2.5 Floor Life

For products with moisture sensitivity level 4, the floor life is 72 hours, or precisely three days. Under factory floor temperature and humidity conditions (<30°C, <60% relative humidity), the parts must be processed and soldered within this specified period of time.

Once the sealed package of the reel is opened and the parts exposed to humidity, they need to be processed within 72 hours (precisely three days) in a reflow soldering process. If this time is exceeded, or the sticker in the sealed package indicates that the goods have been exposed to moisture, the devices need to be pre-baked before the flow solder process. Please refer to *Section 3.3* for instructions on how to pre-bake the components.

3.3 Processing

3.3.1 Moisture Preconditioning

Both encapsulant and substrate materials absorb moisture. JEDEC specification J-STD-020 must be observed to prevent cracking and delamination associated with the "popcorn" effect during solder reflow. The popcorn effect can be described as miniature explosions of evaporating moisture. Baking before processing is required in following cases:

- Humidity indicator card: At least one circular indicator is no longer blue
- Floor life or environmental requirements after opening the seal is opened has been exceeded, e.g. exposure to excessive seasonal humidity.

Recommended baking procedure:

Duration: 48 hours

Temperature: 125°C

Humidity: Below 5%. Desiccant must be placed into the oven to keep humidity low.

Oven: Convection flow oven. Also put desiccant pack into the oven for dehydration.

After work: Put the baked components with desiccant and moisture indicator into a humidity proof bag and use a vacuum hot barrier sealing machine for sealing if not processed within specified floor time. Storage in a nitrogen cabinet or dry box is also a possible approach to prevent moisture intake.

Do not attempt to bake LEA-5 modules contained in tape and rolled up in reels. If baking is necessary first remove the modules from the belt and place them individually onto the oven tray, then bake them at 125°C for 48 hours.

A repeated baking process will reduce the wetting effectiveness of the pad contacts. This applies to all SMT devices.

3.3.2 Soldering Paste

Use of "No Clean" soldering paste is strongly recommended, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste: LFSOLDER TLF-206-93F (Tamura Kaken (UK) Ltd.)

Alloy specification: Sn 95.5/ Ag 3.9/ Cu 0.6 (95.5% Tin/ 0.6 % Silver/ 0.6% Copper)

Melting Temperature: 216 - 221°C

Stencil Thickness: 150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.8.2.

The quality of the solder joints on the connectors ('half vias') should meet the appropriate IPC specification.

3.3.3 Reflow Soldering

A convection type-soldering oven is strongly recommended over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the "IPC-7530 Guidelines for temperature profiling for mass soldering (reflow and wave) processes, published 2001".

Preheat Phase

Initial heating of component leads and balls. Residual humidity will be dried out. Please note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: 1 - 4°C/s — If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.
- Time: 60 – 120 seconds — If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End Temperature: 150 - 200°C — If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ Reflow Phase

The temperature rises above the liquidus temperature of 216 - 221°C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above 220°C liquidus temperature: 20 - 40s
- Peak reflow temperature: 230 - 250°C

Cooling Phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 3°C / s

☞ To avoid falling off, the u-blox 5 GPS/GALILEO module should be placed on the topside of the motherboard during soldering.

The final soldering temperature chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc. Exceeding the maximum soldering temperature in the recommended soldering profile may permanently damage the module.

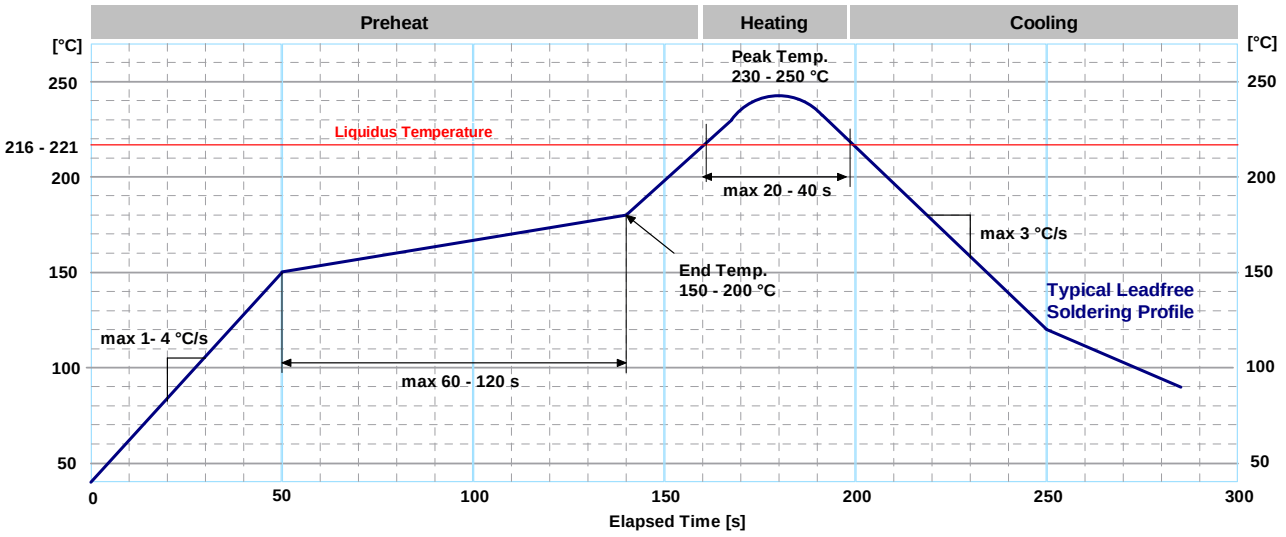


Figure 30: Recommended soldering profile

☞ When soldering leadfree (u-blox 5) modules in a leaded process, check the following temperatures:

- PB- Technology Soaktime: 40-80sec
- Time above Liquidus: 40-90 sec
- Peak temperature: 225-235 °C

☞ LEA-5 modules must not be soldered with a damp heat process.

3.3.4 Optical Inspection

After soldering the LEA-5 module, consider an optical inspection step to check whether:

- The module is properly aligned and centered over the pads
- All pads are properly soldered
- No excess solder has created contacts to neighboring pads, or possibly to pad stacks and vias nearby.

3.3.5 Cleaning

In general, cleaning the populated modules is strongly discouraged. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

The best approach is to use a "no clean" soldering paste and eliminate the cleaning step after the soldering.

3.3.6 Repeated Reflow Soldering

Only a single reflow soldering process is encouraged for boards with a LEA-5 module populated on it. The reason for this is the risk of the module falling off due to high weight in relation to the adhesive properties of the solder.

3.3.7 Wave Soldering

Base boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. Only a single wave soldering process is encouraged for boards populated with LEA-5 modules.

3.3.8 Hand Soldering

Hand soldering is allowed. Use a soldering iron temperature setting of "7" which is equivalent to 350°C and carry out the hand soldering according to the IPC recommendations / reference documents IPC7711.

Place the module precisely on the pads. Start with a cross-diagonal fixture soldering (e.g. pins 1 and 15), and then continue from left to right.

3.3.9 Rework

The LEA-5 module can be unsoldered from the baseboard using a hot air gun.

Avoid overheating the module.

After the module is removed, clean the pads before placing and hand-soldering a new module.

Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

3.3.10 Conformal Coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

These materials affect the HF properties of the GPS module and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating.

☞ Conformal Coating of the module will void the warranty.

3.3.11 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the LEA-5 module before implementing this in the production.

☞ Casting will void the warranty.

3.3.12 Grounding Metal Covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interferences and noise.

☞ u-blox makes no warranty for damages to the LEA-5 module caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

3.3.13 Use of Ultrasonic Processes

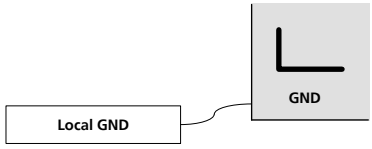
Some components on the LEA-5 module are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding etc.) may cause damage to the GPS Receiver.

☞ u-blox offers no warranty against damages to the LEA-5 module caused by any Ultrasonic Processes.

3.4 ESD Handling Precautions

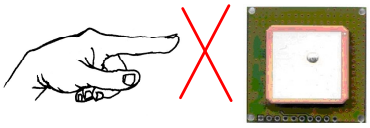
GPS receivers are Electrostatic Sensitive Devices (ESD) and require special precautions when handling. Particular care must be exercised when handling patch antennas, due to the risk of electrostatic charges. In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the receiver:

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB shall always be between the local GND and PCB GND.

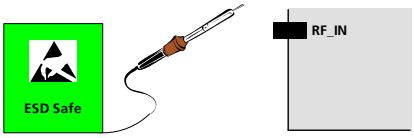


- When handling the RF pin, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna ~10pF, coax cable ~50-80pF/m, soldering iron, …)

- To prevent electrostatic discharge through the RF input do not touch the mounted patch antenna.



- When soldering RF connectors and patch antennas to the receiver's RF pin, make sure to use an ESD safe soldering iron (tip).



Failure to observe these precautions can result in severe damage to the GPS receiver!

For ESD protection design measures see Section 2.10.

4 Product Testing

4.1 u-blox In-Series Production Test

u-blox focuses on high quality for its products. To achieve a high standard it's our philosophy to supply fully tested units. Therefore at the end of the production process, every unit is tested. Defective units are analyzed in detail to improve the production quality.

This is achieved with automatic test equipment, which delivers a detailed test report for each unit. The following measurements are done:

- Digital self-test (Software Download, verification of FLASH firmware, etc.)
- Measurement of voltages and currents
- Measurement of RF characteristics (e.g. C/No)

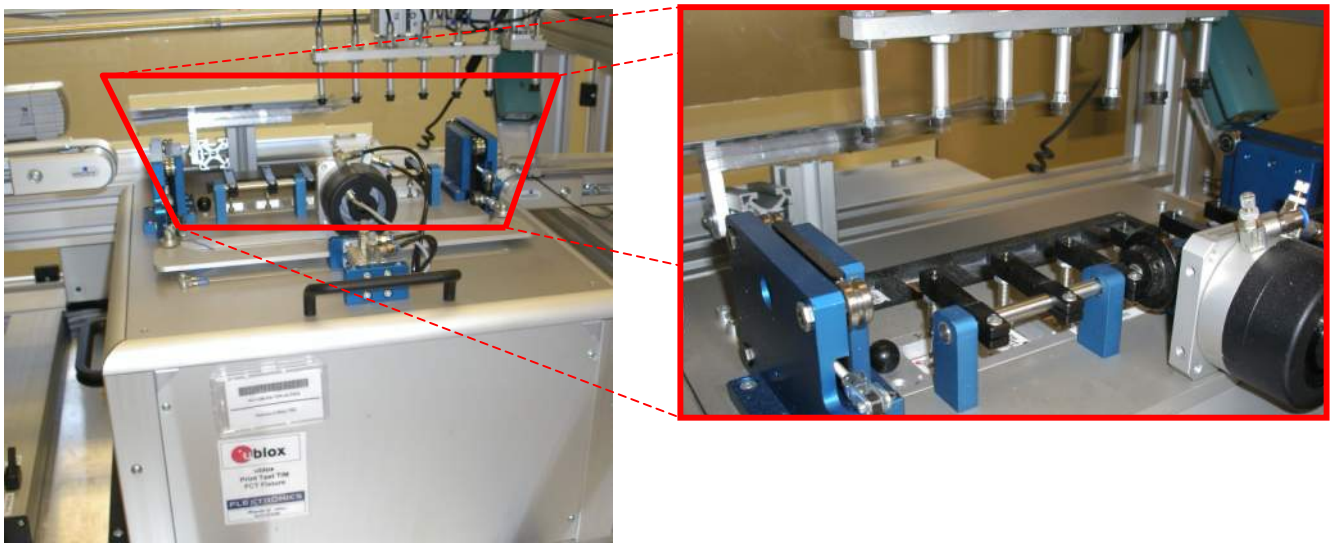


Figure 31: Automatic Test Equipment for Module Tests

4.2 Test Parameters for OEM Manufacturer

Because of the testing done by u-blox (with 100% coverage), it is obvious that an OEM manufacturer doesn't need to repeat firmware tests or measurements of the GPS parameters/characteristics (e.g. TTFF) in their production test.

An OEM Manufacturer should focus on

- Overall sensitivity of the device (including antenna, if applicable)
- Communication to a host controller

4.3 System Sensitivity Test

The best way to test the sensitivity of a GPS device is with the use of a 1-channel GPS simulator. It assures reliable and constant signals at every measurement.

Figure 32: 1-channel GPS simulator

u-blox recommends the following Single-Channel GPS Simulator:

- Spirent GSS6100
  Spirent Communications Positioning Technology
  (previously GSS Global Simulation Systems) www.positioningtechnology.co.uk

4.3.1 Guidelines for Sensitivity Tests

1. Connect a 1-channel GPS simulator to the OEM product
2. Choose the power level in a way that the "Golden Device" would report a C/No ratio of 38-40 dBHz
3. Power up the DUT (Device Under Test) and allow enough time for the acquisition
4. Read the C/No value from the NMEA GSV or the UBX-NAV-SVINFO message (e.g. with u-center)
5. Compare the results to a "Golden Device" or a u-blox 5 Evaluation Kit.

4.3.2 'Go/No go' tests for integrated devices

The best test is to bring the device to an outdoor position **with excellent sky view** (HDOP < 3.0). Let the receiver acquire satellites and compare the signal strength with a "Golden Device".

☞ As the electro-magnetic field of a redistribution antenna is not homogenous, indoor tests are in most cases not reliable. These kind of tests may be useful as a 'go/no go' test but not for sensitivity measurements.

Appendix

A Migration to u-blox 5 Receivers

Migrating ANTARIS®4 to a u-blox 5 receiver module is a fairly straightforward procedure. Nevertheless there are some points to be considered during the migration.

☞ Not all of the functionalities available with ANTARIS®4 are supported by u-blox 5. These include:

- FixNow Mode
- Low Power Modes
- RTCM
- UTM

A.1 Migration from LEA-4 to LEA-5

The pin-outs of LEA-4 and LEA-5H/T differ slightly. Table 10 and Table 11 compare the modules and highlight the differences to be considered.

Pin	LEA-4H/LEA-4P/LEA-4T		LEA-5H/LEA-5T		Remarks for Migration
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
1	**Reserved**	VDDIO level I/O; not connected	**SDA2**	NC	
2	**Reserved**	VDDIO level I/O; not connected	**SCL2**	NC	
3	**TXD1**	VDDIO level I/O	**TxD1**	Output	
4	**RXD1**	VDDIO level I/O	**RxD1**	Input	Leave open if not used.
5	**VDDIO**	1.65 – 3.60V	**NC**	Connect to VCC	Can be left open, but connection to VCC is recommended for compatibility reason (e.g LEA-5Q). With LEA-5H the I/O voltage is always VCC.
6	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.60V	Extended power supply range, higher peak supply current.
7	**GND**	GND	**GND**	GND	No difference
8	**VDD18OUT**	NC	**VCC_OUT**	NC	Internally connected to VCC, if you have circuitry connected to this pin, check if it withstands the VCC voltage.
9	**Reserved**	NC	**Reserved**	NC	
10	**RESET_N**	1.8V	**RESET_N**	NC	Input only, do not drive high. Internal pull up to VCC.
11	**V_BAT**	1.50 – 3.6V	**V_BCKP**	1.4 – 3.6V	Wider voltage range but needs more current. Check your backup supply, regarding the higher consumption.
12	**BOOT_INT**	NC	**Reserved**	NC	do not drive low.
13	**GND**	GND	**GND**	GND	No difference
14	**GND**	GND	**GND**	GND	No difference
15	**GND**	GND	**GND**	GND	No difference
16	**RF_IN**	RF_IN	**RF_IN**	RF_IN	No difference
17	**GND**	GND	**GND**	GND	No difference
18	**VCC_RF**	VCC - 0.1V	**VCC_RF**	VCC - 0.1V	No difference
19	**V_ANT**	3.0V –5.0V	**V_ANT**	2.7V -5.5V	No difference
20	**AADET_N**	NC	**AADET_N**	NC	
21	**EXTINT1**	NC	**NC**	NC	
22	**Reserved**	NC	**NC**	NC	
23	**Reserved**	NC	**NC**	NC	
24	**VDDUSB**	Connected to GND or VDD_USB	**VDDUSB**	Connected to GND or VDD_USB	Do not leave open. (VDD_USB is 3.3V regulated power supply from VBUS.)
25	**USB_DM**	NC	**USB_DM**	NC	No difference
26	**USB_DP**	NC	**USB_DP**	NC	No difference
27	**EXTINT0**	NC	**EXTINT0**	NC	
28	**TIMEPULSE**	VDDIO level I/O	**TIMEPULSE**	Output	

: Pins to be checked carefully; NC: Not connected

Table 10: Pin-out comparison LEA-4H/LEA-4P/LEA-4T vs. LEA-5H/LEA-5T

Pin	LEA-4A/LEA-4S		LEA-5A/LEA-5S		Remarks for Migration
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
1	**TxD2**	3.0V out	**SDA2**	NC	
2	**RxD2**	1.8 - 5.0V	**SCL2**	NC	
3	**TxD1**	3.0V out	**TxD1**	Output	
4	**RxD1**	1.8 - 5.0V in	**RxD1**	Input	Leave open if not used.
5	**VDDIO**	VCC	**NC**	Connect to VCC	Can be left open, but connection to VCC is recommended for compatibility reason (e.g LEA-5Q).
6	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.60V	Extended power supply range, higher peak supply current.
7	**GND**	GND	**GND**	GND	No difference
8	**VDD18OUT**	1.8V out	**VCC_OUT**	NC	Internally connected to VCC, if you have circuitry connected to this pin, check if it withstands the VCC voltage.
9	**GPSMODE6**	NC (GND or VDD18OUT)	**CFG_COM1**	NC	
10	**RESET_N**	*ACTIVE LOW*	**RESET_N**	NC	Input only, do not drive high. Internal pull up to VCC.
11	**V_BAT**	1.50 – 3.6V	**V_BCKP**	1.4 – 3.6V	Wider voltage range but needs more current. Check your backup supply, regarding the higher consumption.
12	**BOOT_INT**	NC	**Reserved**	NC	do not drive low.
13	**GND**	GND	**GND**	GND	No difference
14	**GND**	GND	**GND**	GND	No difference
15	**GND**	GND	**GND**	GND	No difference
16	**RF_IN**	RF_IN	**RF_IN**	RF_IN	No difference
17	**GND**	GND	**GND**	GND	No difference
18	**VCC_RF**	VCC - 0.1V	**VCC_RF**	VCC - 0.1V	No difference
19	**V_ANT**	3.0V - 5.0V	**V_ANT**	2.7V -5.5V	No difference
20	**AADET_N**	NC (1.8 to 5.0V)	**AADET_N**	NC	
21	**GPSMODE5**	NC (GND or VDD18OUT)	**NC**	NC	
22	**GPSMODE2 GPSMODE2 3**	NC (GND or VDD18OUT)	**NC**	NC	
23	**GPSMODE7**	NC (1.8 to 5.0V)	**NC**	NC	
24	**VDDUSB**	3.0 –3.6V/ GND	**VDDUSB**	Connected to GND or VDD_USB	Do not leave open. (VDD_USB is 3.3V regulated power supply from VBUS.)
25	**USB_DM**	VDDUSB I/O	**USB_DM**	NC	No difference
26	**USB_DP**	VDDUSB I/O	**USB_DP**	NC	No difference
27	**EXTINT0**	NC (1.8 to 5.0V)	**EXTINT0**	NC	
28	**TIMEPULSE**	VDDIO out	**TIMEPULSE**	Output	

: Pins to be checked carefully; NC: Not connected

Table 11: Pin-out comparison LEA-4A/LEA-4S vs. LEA-5A/LEA-5S

B Reference Design

B.1 LEA-5 Smart Antenna

The following design supports all LEA-5 modules on one PCB and features one serial port as well as a USB connection. If USB is not needed some components can be spared.

☞ For this design u-blox provides a complete Smart Antenna Demo Design including Schematic, Gerber Files, PCB blueprint and recommendations. Contact u-blox support for further information. Conditions apply.

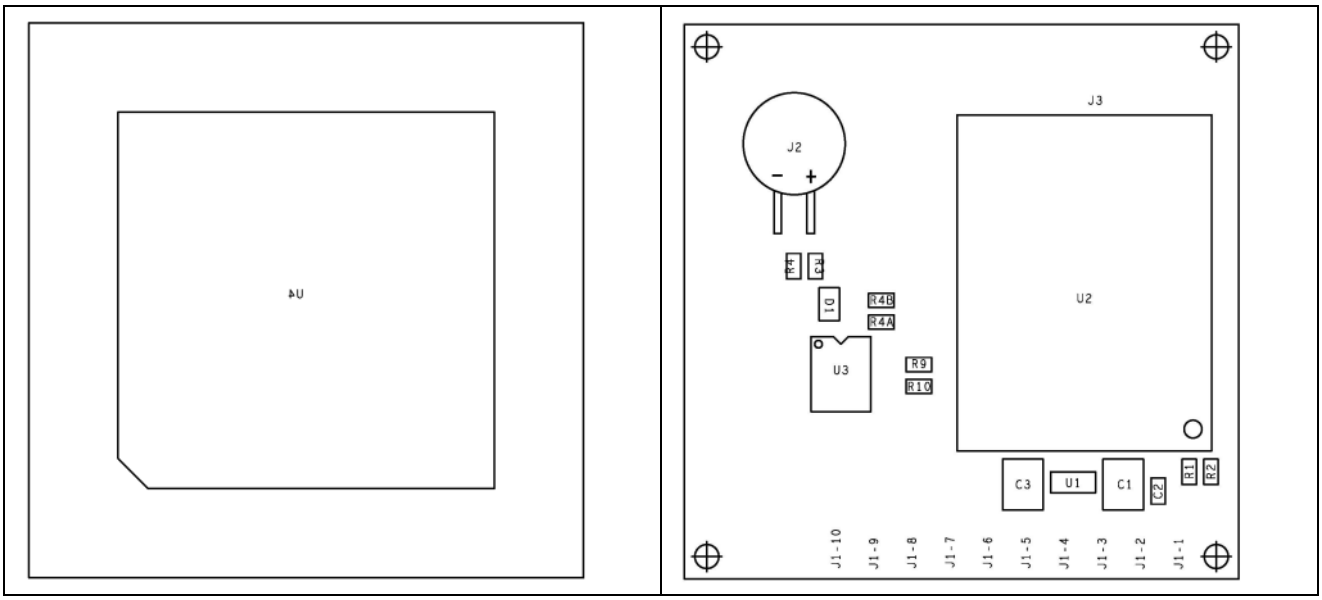


Figure 33: LEA-Smart Antenna (top view/ bottom view)

B.1.1 Schematic

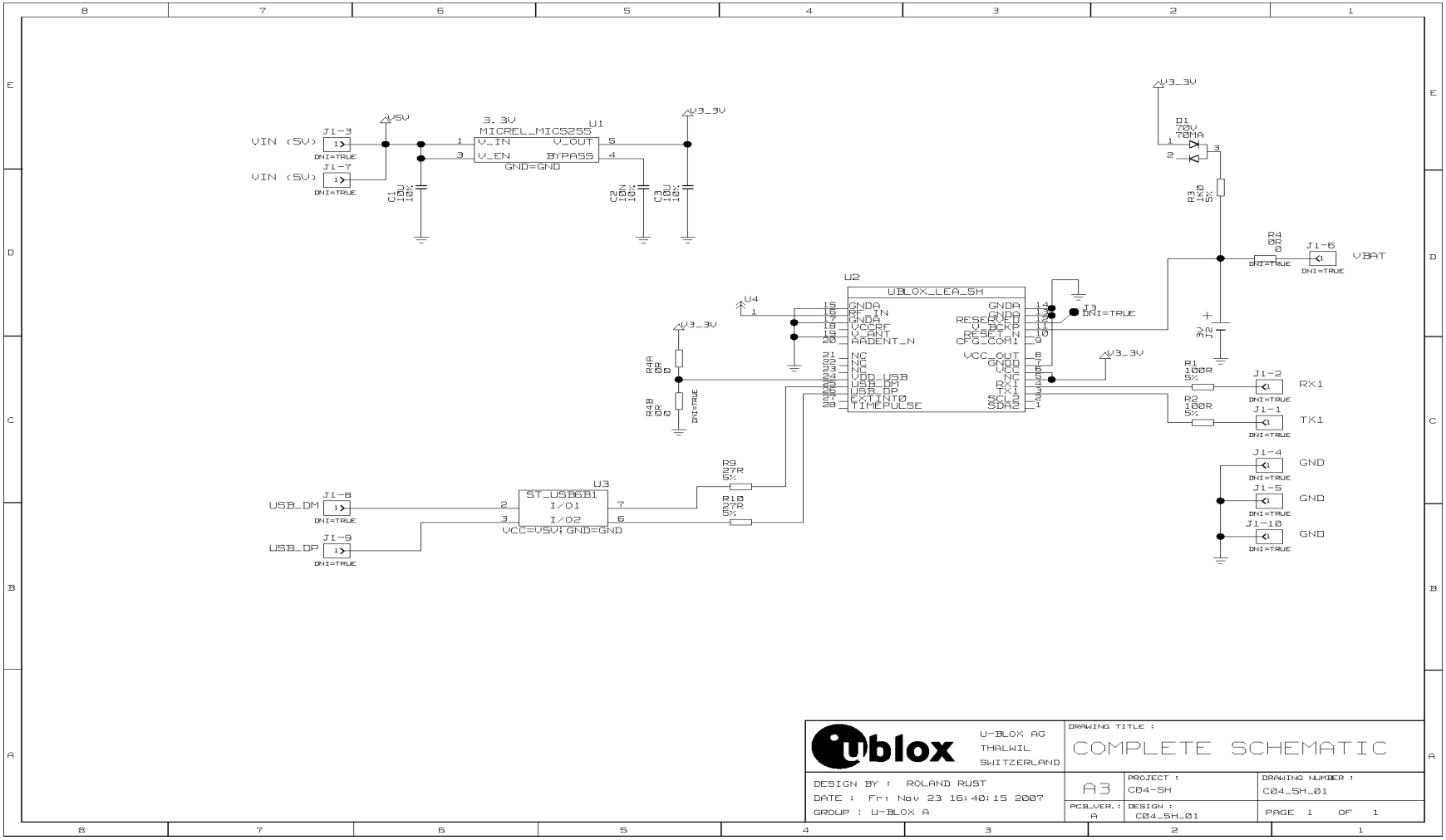


Figure 34: LEA Smart Antenna Schematic

B.1.2 Bill of Material

	Part description	Remarks
C1, C3	CER X5R 1210 10µ 10% 10V ROHS	
C2	CER X7R 0603 10n 10% 25V ROHS	
D1	SCHOTTKY DIODE INFINEON BAS70-04W 70V 70MA ROHS	Only required if optional battery J2 is used.
J2	BATTERY PANASONIC 3V 5MVA ML621S ROHS	Optional. If not used, connect pin J1-6 to battery on motherboard or to GND.
R1 R2	RES THICK FILM CHIP 0603 100R 5% 0.1W ROHS	
R10 R9	RES THICK FILM CHIP 0603 27R 5% 0.1W ROHS	Do not fit if USB is not used.
R3	RES THICK FILM CHIP 0603 1K0 5% 0.1W ROHS	Only required if optional battery J2 is used.
R4	RES THICK FILM CHIO 0603 0R 0.1W ROHS	Only required if optional battery J2 is not used.
R4A	RES THICK FILM CHIP 0603 0R 0.1W ROHS	Fit only if USB is used.
R4B	RES THICK FILM CHIO 0603 0R 0.1W ROHS	Fit only if USB is used.
U1	LOW DROPOUT REGULATOR MICREL MIC5255 3.3V 150MA SOT23 ROHS	
U2	GPS RECEIVER U-BLOX LEA-5H-0-000 ROHS	
U3	USB DATA LINE PROTECTION ST USB6B1 SO8 ROHS	Do not fit if USB is not used
U4	CERAMIC PATCH ANTENNA TH 25mm x 25mm FO=1575 ROHS	e.g. INPAQ PA1575MZ50I4G-13-13/1589

Table 12: Bill of Material

☞ Depending on the required interface (USB or UART), several parts don't have to be fit. The same applies to the backup battery if an external backup supply is available. Refer to Table 12 for the feasible options.

B.1.3 Layout

The layout is designed for a 2-layer **1mm FR4 PCB board**.

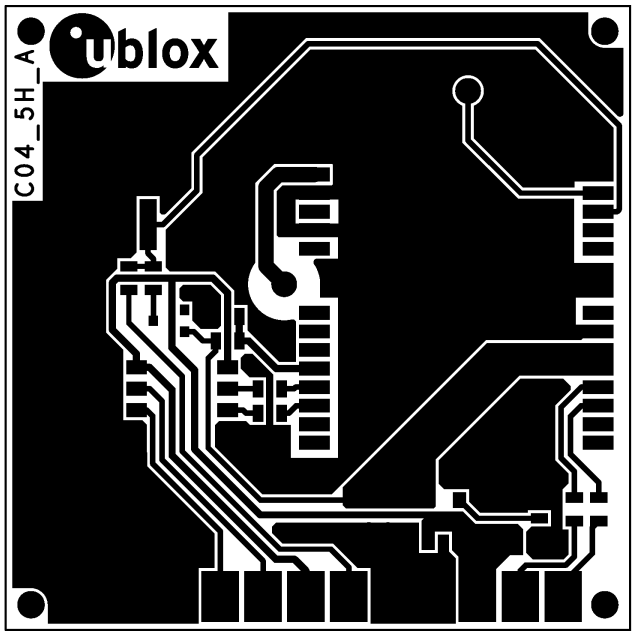


Figure 35: Top Layer

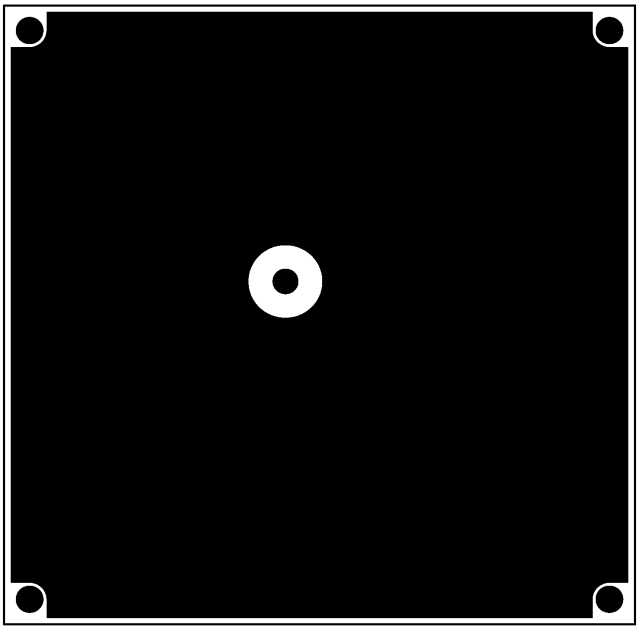


Figure 36: Bottom Layer

C Glossary

BBR	Battery backup RAM
ESD	Electro Static Discharge
GNSS	Global Navigation Satellite System
LNA	Low Noise Amplifier
MSL	Height above Mean Sea Level or Orthometric Height
NMEA 0183	ASCII based standard data communication protocol used by GPS receivers.
PUBX	u-blox proprietary extension to the NMEA protocol
UBX	File extension for u-center log file or short form for the UBX protocol
UBX Protocol	A proprietary binary protocol used by the u-blox GPS technologies

Related Documents

[1] u-blox 5 Protocol Specification, Docu. No GPS.G5-X-07036

[2] GNSS Compendium, Doc No GPS-X-02007

[3] LEA-5 Data Sheet, Doc No GPS.G5-MS5-07026

[4] DDC Implementation Application Note, Docu. No GPS.G5-X-08023

[5] SPI Implementation Application Note, Docu. No GPS.G5-X-08028

[6] GPS Antenna Application Note, Docu. No GPS-X-08014 (to be released 01/2009)

[7] u-blox 5 Power Management Application Note, Docu. No GPS.G5-CS-08022 (to be released 01/2009)

All these documents are available on our homepage (http://www.u-blox.com).

For regular updates to u-blox documentation and to receive product change notifications please register on our homepage.

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